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HIGH FREQUENCY ANALOG LSI DEVELOPMENT.(U)
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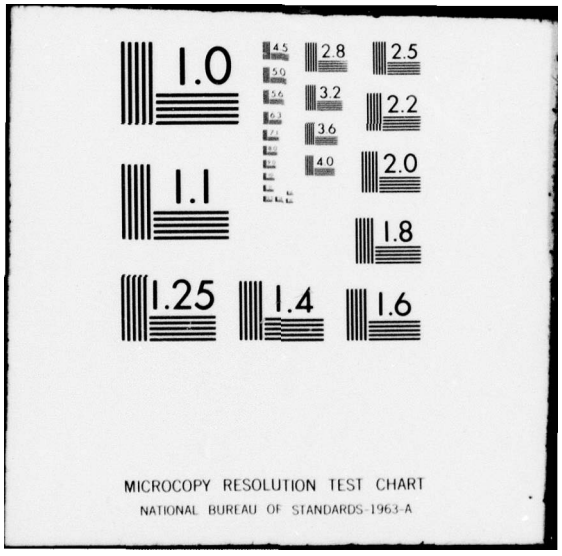
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Demodulator	Computer Aided Analysis	

20. ABSTRACT (Continue on reverse side if necessary and identify by block number)

This report documents all analysis and design efforts undertaken in the first year of a three-year program aimed toward utilizing OAT fabrication technology to develop building block circuits appropriate to the satisfaction of system requirements for communication networks operating through L-band. Basic circuit techniques for LSI are discussed in depth, as are the design and fabrication of universal RF building blocks. The results of a GPS receiver system/module interface study are presented. Finally, the

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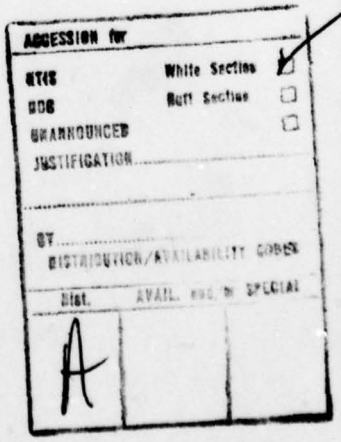
fabricated realization of a GPS test chip is developed and completely defined.



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HIGH FREQUENCY ANALOG LSI DEVELOPMENT

October 1, 1978

YEARLY INTERIM REPORT
for Period 1 September 1977 — 1 September 1978

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PREFACE

This interim report documents the results of the first year effort performed under Navy Contract N00123-77-C-1045. The work is sponsored by the Naval Electronic Systems Command, Washington, D.C., by Mr. Nathan Butler and Mr. Larry Sumney of the Electronics Technology Division, ELEX 304. The contract monitor is Mr. C. A. West, Naval Ocean Systems Center, Code 923, San Diego, California. The work is being conducted by the Microelectronics Center of TRW Defense and Space Systems Group. The principal TRW investigator and author of this report is Dr. John Choma, Jr., who reports directly to Dr. Barry Dunbridge, Director of the Microelectronics Center.

The author thanks A. Cosand, who contributed substantially to this report and who is responsible for much of the layout and design work documented herewith. He also thanks L. Fletcher for expediting the administrative details pertinent to ensuring successful completion of all phases of RFLSI research and development during the past year.

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CONTENTS

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1.0 INTRODUCTION

In September of 1977, TRW DSSG undertook a three year program to use the oxide aligned transistor (OAT) fabrication technology to develop circuit techniques and building block circuits appropriate to the satisfaction of system requirements for communication networks operating at signal frequencies through L-band. The program, sponsored by the Naval Ocean Systems Center, under contract N000123-77-C-1045, is configured in terms of six distinct tasks.

Both Tasks 1 and 3 of this program are virtually complete at this juncture. The results of TASK 1 efforts are documented separately and accordingly, this yearly interim report addresses TASK 3 work almost exclusively. TASK 3 focuses on the design, development, and fabrication of a GPS test chip. Section 4.0 defines and discusses this chip, while two earlier sections document the results of work performed in support of establishing a finalized design for the test chip. In Section 2.0, for example, the initial conception and subsequent optimization of the GPS chip system architecture is presented. Section 3.0 gives the results of company sponsored research and development aimed toward establishing GPS test chip feasibility through design and fabrication of a so-called RFE test chip. A study of the measured performance of circuits embedded in this chip proved invaluable in the design of substantially improved circuits for incorporation in the GPS test chip.

Section 5.0 briefly describes the nature of continuing near term research and development activities. Since the design of circuits discussed in Section 4.0 rely heavily on the fruits of TASK 1, the TASK 1 report is included as an appendix.

It is appropriate to underscore the fact that the GPS test chip is a benchmark for the state-of-the-art in monolithic bipolar LSI communication circuits. Substantial justification can be offered to demonstrate its uniqueness in the world of custom LSI. First and foremost, the chip contains circuits for <u>all</u> analog and digital functions indigenous to GPS. This is to say that the code tracking loop, including on-chip code reclocking and both data and clock buffering are incorporated,

in addition to the traditional amplification, detection, mixing, and oscillation functions of a communication circuit. Second, RF amplification of signal frequencies through L-band are realized on chip without resorting to hybrid forms of circuit realization. The RF amplifier utilizes inter-stage lossless matching networks to achieve the desired frequency response, and the inductors of these matching networks are also implemented on chip. Even an operational amplifier is synthesized on chip for signal detection purposes. Finally, a less dramatic feature of the GPS chip is that all of its circuits exploit extremely sophisticated computer aids for design and concomitant realistic device parameter extraction techniques. In particular, devices are characterized for computer-oriented design by measuring their scattering parameters and quiescent characteristics in an environment that closely replicates the operating conditions of the circuit into which they are ultimately embedded.

2.0 GPS CHIP SYSTEM ARCHITECTURE

2.1 Initial Conception[1]

Figure 2-1 is the initially recommended system schematic for the GPS receiver chip. The philosophy underlying the recommended system schematic reflects the following viewpoints and assumptions. First, consistent with the overall building block approach for RFLSI technology, identical circuits are replicated where possible, rather than implementing custom designs for each block. Second, risk is reduced by using proven analog multiplier designs fabricated earlier. Third, excess gain is provided in two locations to help ensure that the total gain in both signal paths meets specifications even if the preamplifier gain is low or the mixer conversion loss high due either to minor design or processing errors. For the remainder of this discussion, the upper four circuits in Figure 2-1 (A_1, A_2, M_1, and M_2) are referred to as the "signal path," and the lower three (M_1, M_2, and A_2) circuits are termed the code tracking path.

2.1.1 Signal Path Gain

The overall gain required in the signal path is 43dB with a 15dB AGC range; i.e., 28-43dB total gain. The gain is partitioned as indicated in Figure 2-2. The gain of A_1 is chosen to amplify the input to the level at which the analog multiplier is well behaved. Amplifier A_2 nominally has a fixed gain of 18dB. However, as there are uncertainties about the exact mixer conversion loss, and since A_1 can conceivably have less than the desired 30dB gain, approximately 10dB of excess gain has been designed into A_2. Table 2-1 lists the specifications for amplifier A_2.

DC blocks at both inputs to M_1 are recommended, since the anti-jam (A/J) performance of the receiver is critically dependent on the balance of this circuit.

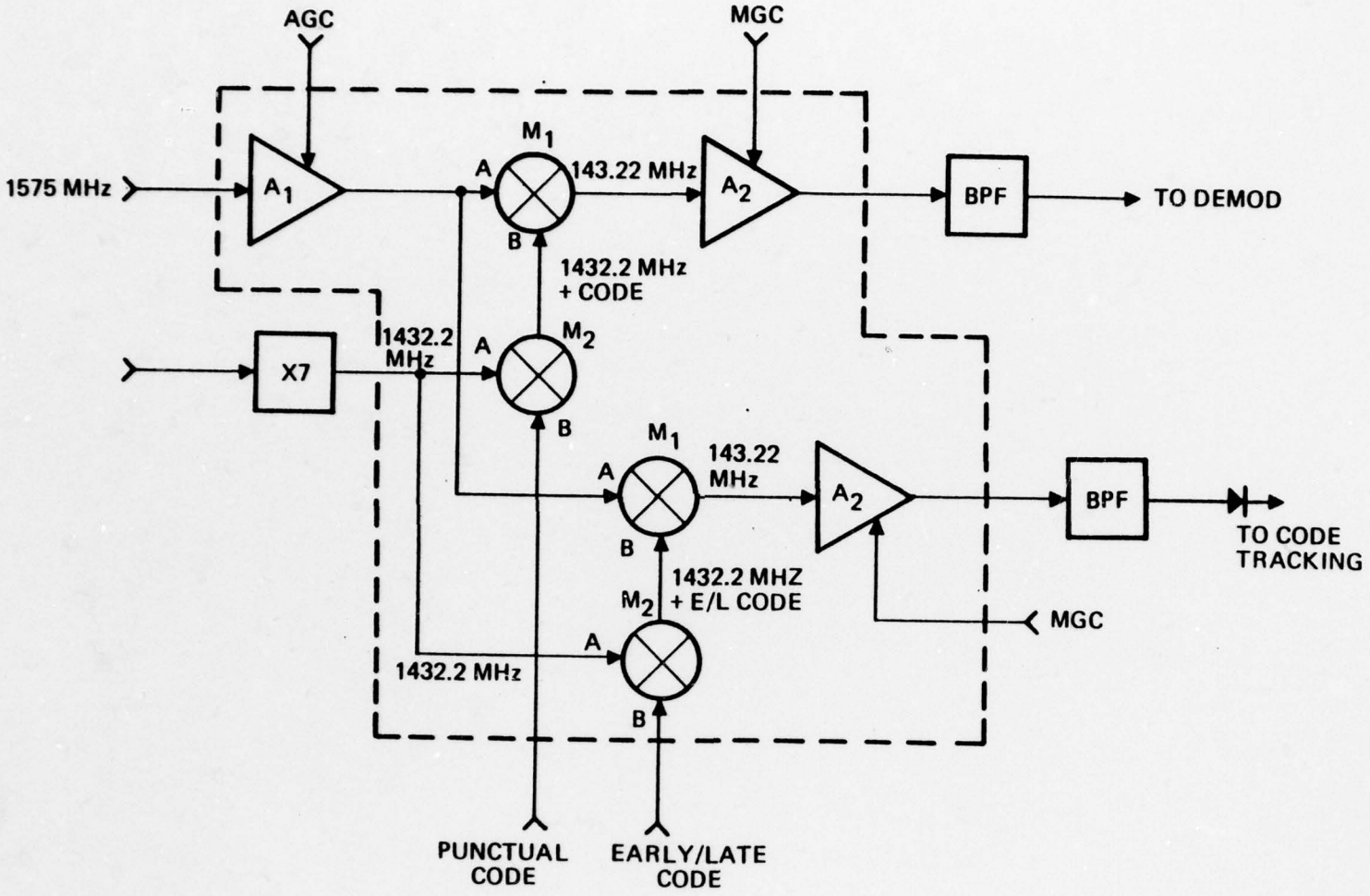


Figure 2-1 GPS Chip Schematic

Dotted enclosure system refers to circuits fabricated monolithically.

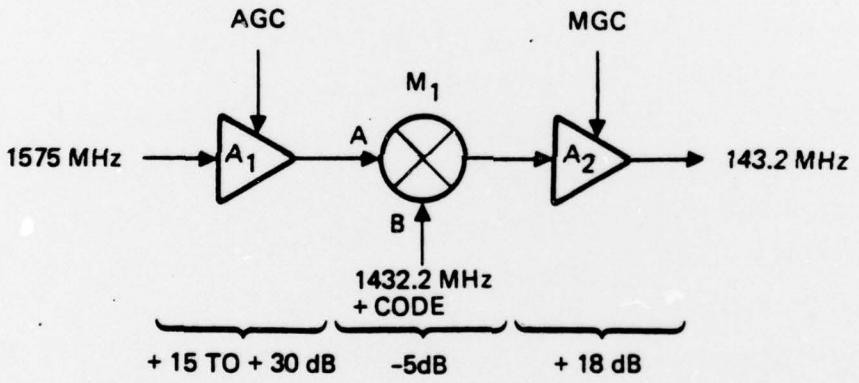


Figure 2-2 Signal Path Gain Distribution

TABLE 2-1 AMPLIFIER A_2 SPECIFICATIONS

INPUT:	143.22 MHz ± 20 MHz (1dB B.W.) -51 to -30dBm Balanced, Compatible with M_1 Output
GAIN:	18dB nominal -13dB to 28dB with manual gain control
OUTPUT:	143.22 MHz ± 20 MHz (1dB B.W.) -33 to -12dBm 50 ohms, Single Ended

2.1.2 Signal Path Processing Gain

Mixer M_1 performs three functions in the signal path. It downconverts the received signal to the 143 MHz IF, it despreads the received spread spectrum signal, and it spreads any jamming signal present within the input bandwidth. The signal processing gain of mixer M_1 is theoretically equal to the ratio of the input code clock frequency to the data rate:

$$\text{Signal Processing Gain} = 10 \text{ Log } \frac{(10.23 \text{ MHz})}{(50 \text{ Hz})} = 53\text{dB}.$$

The receiver input jammer to signal ratio (J/S) is 40dB, and the Costas loop can operate at a J/S ratio of -3dB, so there is 10dB of signal processing gain margin available for hardware implementation loss.

The most likely source of loss of signal processing gain is imperfect carrier suppression in the modulation processes of mixers M_1 and M_2. Assume for a moment that each mixer is capable of providing 50dB of carrier suppression, and that the J/S ratio at input (A) of M_1 is 40dB. To determine the output J/S ratio, the three cases illustrated in Figure 2-3 must be examined. In Figure 2-3a, the input signal and the code are multiplied and 20dB of conversion gain is added, giving an output signal level of -70dBm. In Figure 2-3b, the jammer and code are multiplied, 50dB of suppression is assumed, and the 20dB conversion gain is added, giving a jammer output level of -80dBm. Finally, in Figure 2-3c, the jammer and unsuppressed local oscillator signals are multiplied and the 20dB gain added to give a second component of the jammer output signal at -80dBm. Thus, the total jammer output level is -77dBm, giving a J/S ratio of -7dB, or a processing gain of 47dB.

This discussion is offered for the purpose of illustrating the fact that while the processing gain is theoretically the ratio of the code to data rates, in this receiver it is more likely to be dominated by the mixer carrier suppression. It can be seen from the previous example that the mixer carrier suppression must be $\geq$ 46dB if the receiver is to meet A/J specifications.

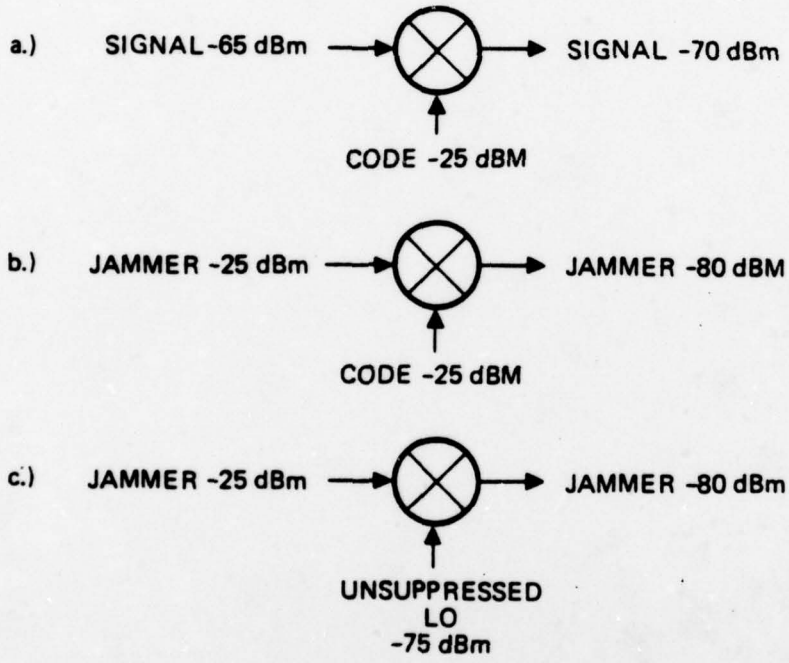


Figure 2-3 Components of J/S Ratio

Inadequate carrier suppression has two possible sources: leakage or lack of isolation through the mixers, and imperfect modulation due to mixer imbalance. Leakage should result in common mode, rather than differential mode, signals; therefore, leakage should not pose significant problems so long as the common mode rejection ratio (differential mode gain divided by common mode gain) of the M_1/A_2 combination can be maintained at greater than 53dB. Previous mixer measurements indicate a CMRR of about 55dB, and the amplifier A_2 should improve this still further.

The second source of inadequate carrier suppression is imbalance in the multipliers and deviation from perfect multiplication. To obviate this problem, the B input of mixer M_2 is DC coupled, and provisions are made for introducing a DC offset voltage at this point to allow suppression of the carrier output of M_2. (This is the technique usually adopted in microwave receivers.) The specifications for mixer M_2 are listed in Table 2-2. A conversion gain factor of k_2 = 20dB is assumed.

2.1.3 Code Tracking Loop

The code tracking loop operates by comparing the correlation gain of the punctual code and an early code against the correlation gain of the punctual code and a late code. The punctual code is by definition, the code as received. The early code is identical to the punctual code, but is is advanced in time by one-half a code clock period. The late code is retarded in time by one-half a code clock period. Figure 2-4 depicts the system schematic diagram of the code tracking loop. Figure 2-5a shows the punctual code, while Figure 2-5b offers a second code that is first early and then late.

The transition between early and late is made at a rate of τ_{REF}^{-1}, which is of the order of a few kHz. During the time intervals when the punctual and early/late code states are the same, the correlation gain of mixer M_2 and bandpass filter is given by the ratio of the code rate to the filter bandwidth:

$$\text{Correlation Gain} = 10 \text{ Log } \frac{(10.23 \text{ MHz})}{(20 \text{ kHz})} = 27\text{dB}.$$

TABLE 2-2 MIXER M_2 SPECIFICATIONS

INPUT A: 1432.2 MHz $\pm$ 5 MHz -25dBm
Balanced, Compatible with X 7 Output, AC Coupled

INPUT B: Code at 1.023 or 10.23 MBPS -20dBm
Balanced, DC Coupled, 2K ohms

OUTPUT: 1432.2 MHz $\pm$ 20 MHz -25dBm
Balanced, Compatible with M_1 Input, AC Coupled

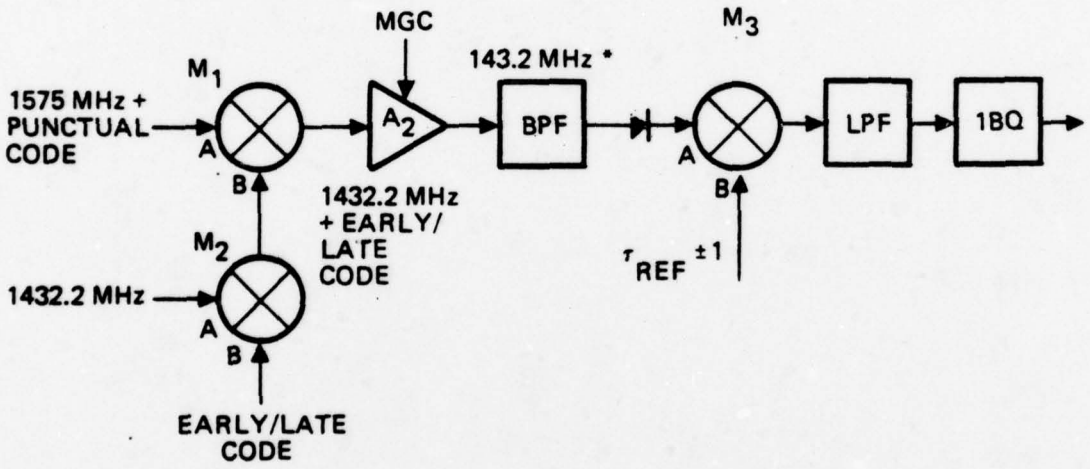


Figure 2-4 Diagrams of Code Tracking Loop

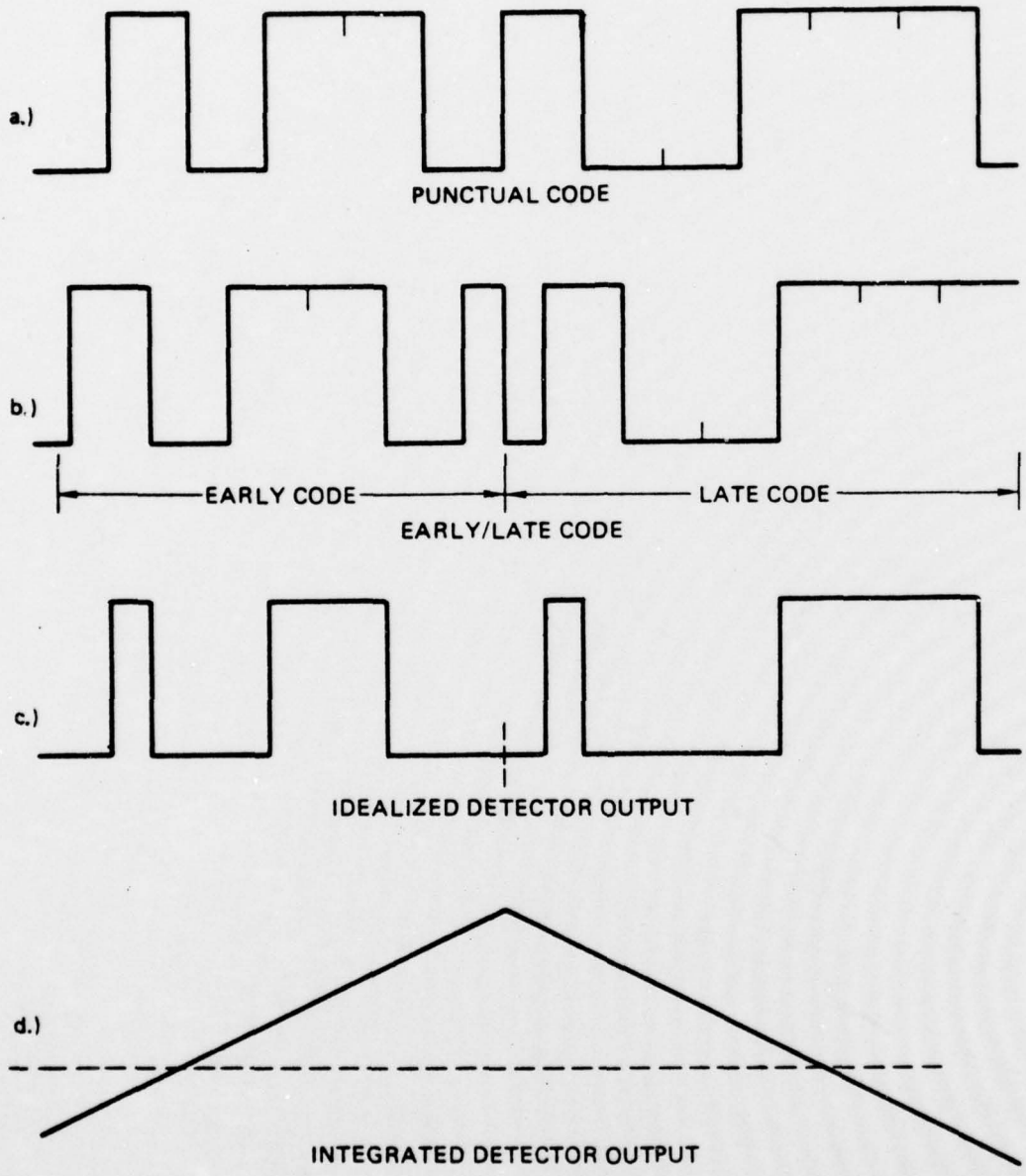


Figure 2-5 Code Tracking Circuit Waveforms

When the punctual and early/late codes are opposite, the correlation gain is zero. If the bandpass filter output is detected, a waveform similar to the one shown in Figure 2-5c results. Now if the detector output is multiplied by +1 when the early code is present and -1 when the late code is present and then integrated over a period that is long compared to the code rate, the waveform shown in Figure 2-5d is generated. If the early and late codes are equally displaced in time from the punctual code, the time average value of the waveform in Figure 2-5d is zero. If the early code overlaps the punctual code longer than the late code, the average value of the aforementioned waveform is positive.

The waveform in Figure 2-5d contains all of the information necessary to lock the code tracking loop. There are a number of options for the next circuit, and those options can be part of an RFLSI chip or part of the microprocessor. Consistent with earlier work[1], the next circuit is a one bit quantizer clocked at 100 τ_{REF}^{-1}. The quantizer is used to fill an accumulator upwards from midrange when the waveform in Figure 2-5d is positive and downwards from midrange when this signal is negative. The time intervals during which the Figure 2-5d signal is positive and negative is thus measured. When the accumulator overflows in either direction, the local code generator clock is advanced or retarded.

The system implementation of these functions is shown in Figure 2-4. Mixer M_1 performs the correlation of the early/late code with the punctual code, and downconverts the input frequency to 143 MHz. Note that signals must be routed off chip only once for both the bandpass filter and detector diode. Amplifier A_2 in the code tracking loop is identical to amplifier A_2 in the signal path, and here the MGC (manual gain control) is used to set the detector diode output level. The only function of mixer M_3 is to multiply the diode's output by +1 when the early/late is early, and -1 when the early/late code is late. The low pass filter bandwidth is well below 143 MHz, and well above τ_{REF}^{-1}. The one bit quantizer can be a fairly simple clocked comparator circuit whose output is compatible with microprocessor input levels.

2.2 Final Form

The final form of the system schematic diagram appears in Figure 2-6. It differs from the initially conceived diagram of Figure 2-1 in the following respects.

1. Mixers M_1 and M_2 in Figure 2-1 are coalesced into a single, three input mixer, M_{1a} and M_{1b}. The new configuration is superior to the classical realization in that it consumes less power, has faster time of response characteristics, and requires less chip area for circuit implementation.

2. Circuitry for the code tracking loop is implemented on chip. Included in this circuitry is a linear detector for the 143 MHz signal, a polarity reversing switch (M_2), an operational amplifier which, when utilized in conjunction with an off-chip capacitor and resistor, serves as a low pass filter for the detected signal, and finally, a comparator (A_4).

3. The input buffer (A_5) converting the single ended local oscillator signal to the differential voltage required by the mixers is now explicitly shown.

4. A reclocking register has been added to ensure that the digital signals supplied to the mixers have equal pulse widths during high and low output voltage intervals, and equal rise and fall times. The register also ensures minimally distorted differential signal drives for the mixers.

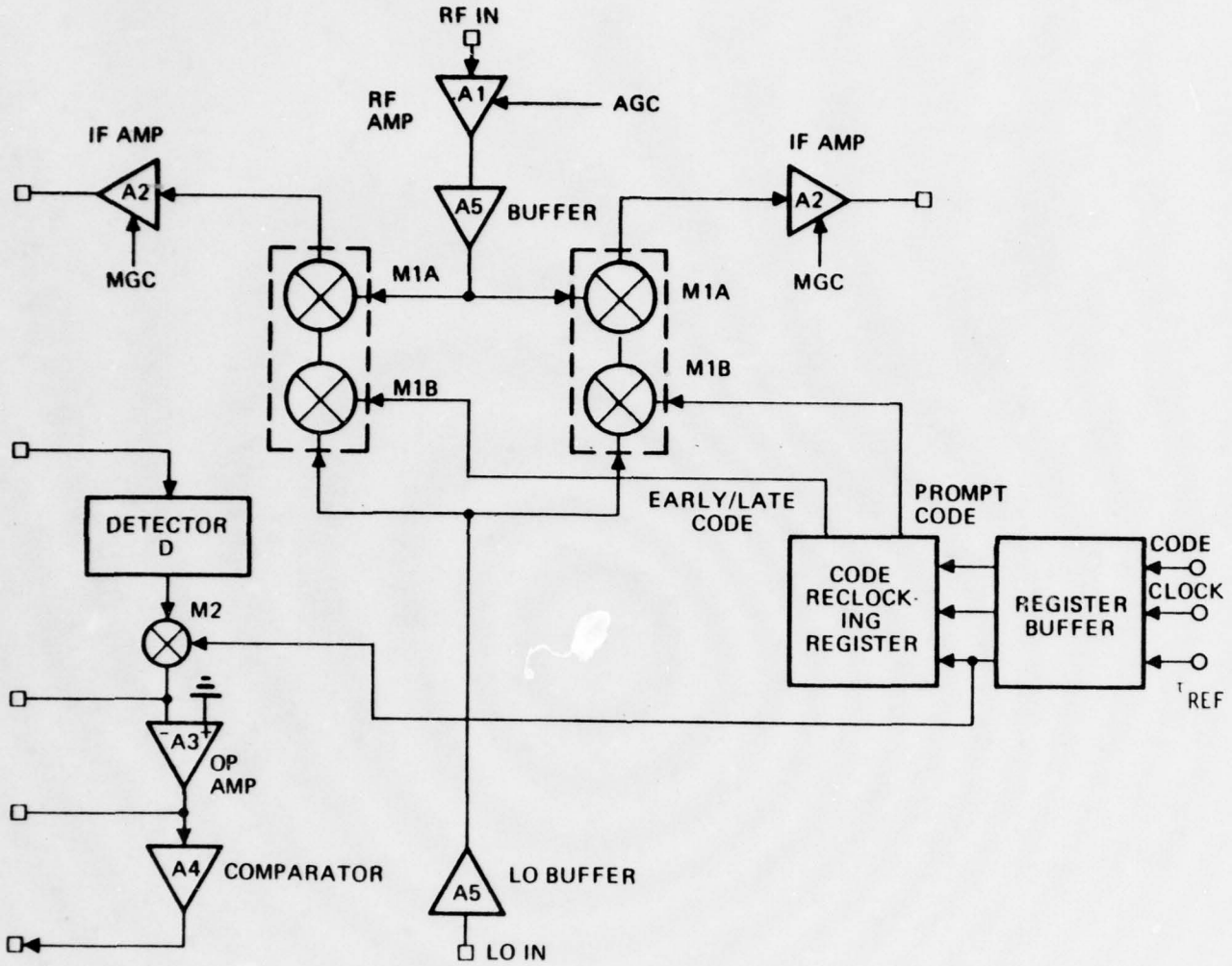


Figure 2-6 Final System Schematic Diagram of GPS Chip

3.0 RFE-1 TEST CHIP

Under a company internal research and development program (IRAD), a test chip was fabricated for the purpose of evaluating building block circuits amenable to utilization in a monolithic GPS receiver. The chip, a microphotograph of which is offered in Figure 3-1, includes two types of RF amplifiers, a phase logic demodulator, a phase detector, and a voltage controlled oscillator.

3.1 RFE-1 RF Amplifier

The two amplifier designs on the RFE chip are shown in Figures 3-2 and 3-3. The only difference between the two designs is the load on the collectors of transistors T12 and T13. For the amplifier in Figure 3-2, referred to as the inductor amplifier, collector loads consist of a resistor in series with an inductor physically realized with a metallized spiral inductor. For the amplifier in Figure 3-3, referred to as the diode amplifier, the collector loads consist of a resistor in series with a transistor-resistor combination which behaves like an inductive load. Both circuits have been tested, and a sample of the test fixture utilized in the inductor amplifier case is pictured in Figure 3-4.

3.1.1 Test Results

The frequency responses of each of three samples of the RF inductor amplifier are given in Figures 3-5 through 3-7, respectively. Similar responses were obtained for samples of the diode version of this amplifier. In all cases, the maximum gain is in the range of 40-to-50dB, and inductively induced peaking is observed below approximately 375 MHz. The overall 3dB bandwidth is in the range of 400-to-600 MHz.

The results of noise characterizations indicate a minimum noise figure of 0.8dB at 200 MHz. The noise figure rises sharply both above and below 200 MHz.

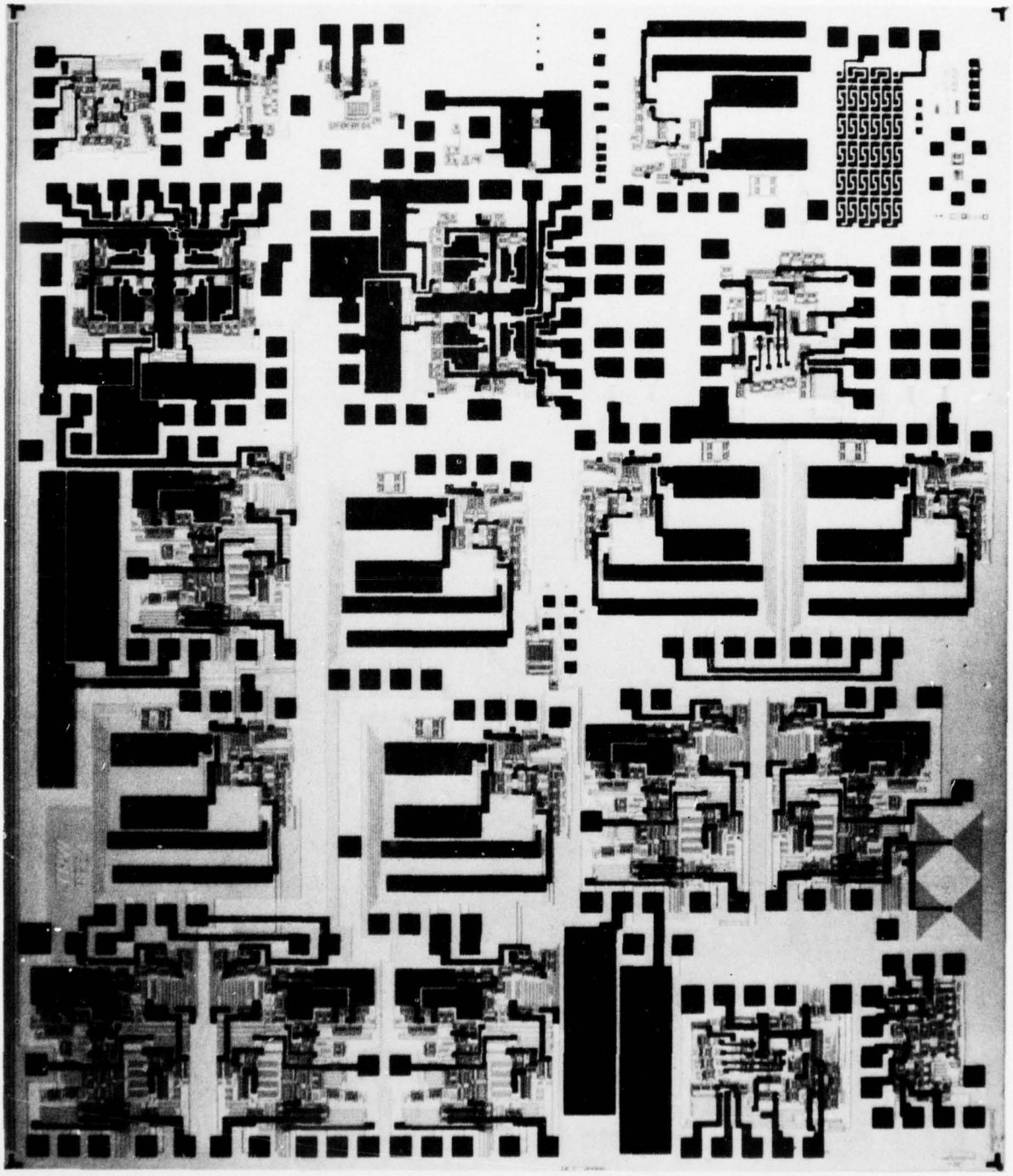


Figure 3-1 Microphotograph of RFE-1 Test Chip

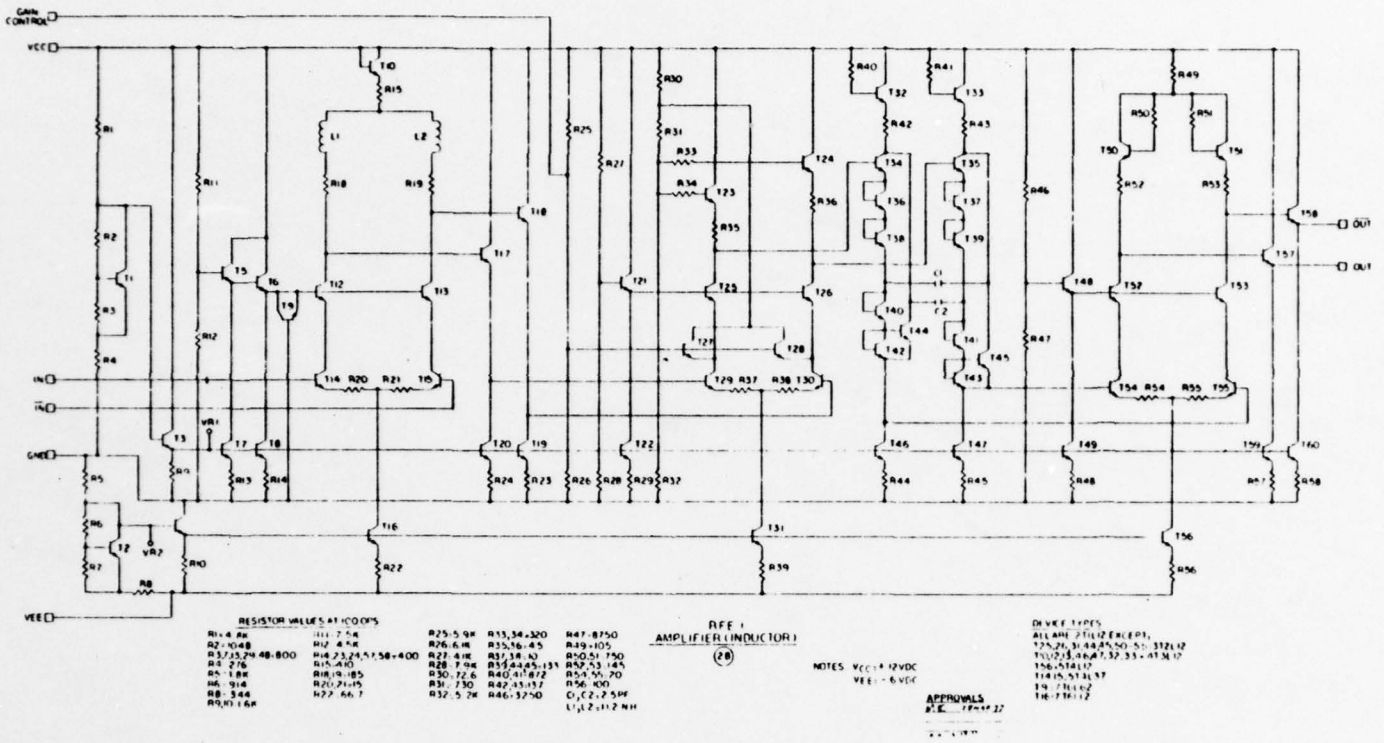


Figure 3-2 RF Amplifier Schematic
Uses Metallization Spiral Inductors (L_1 and L_2) for Shunt Peaking Purposes.

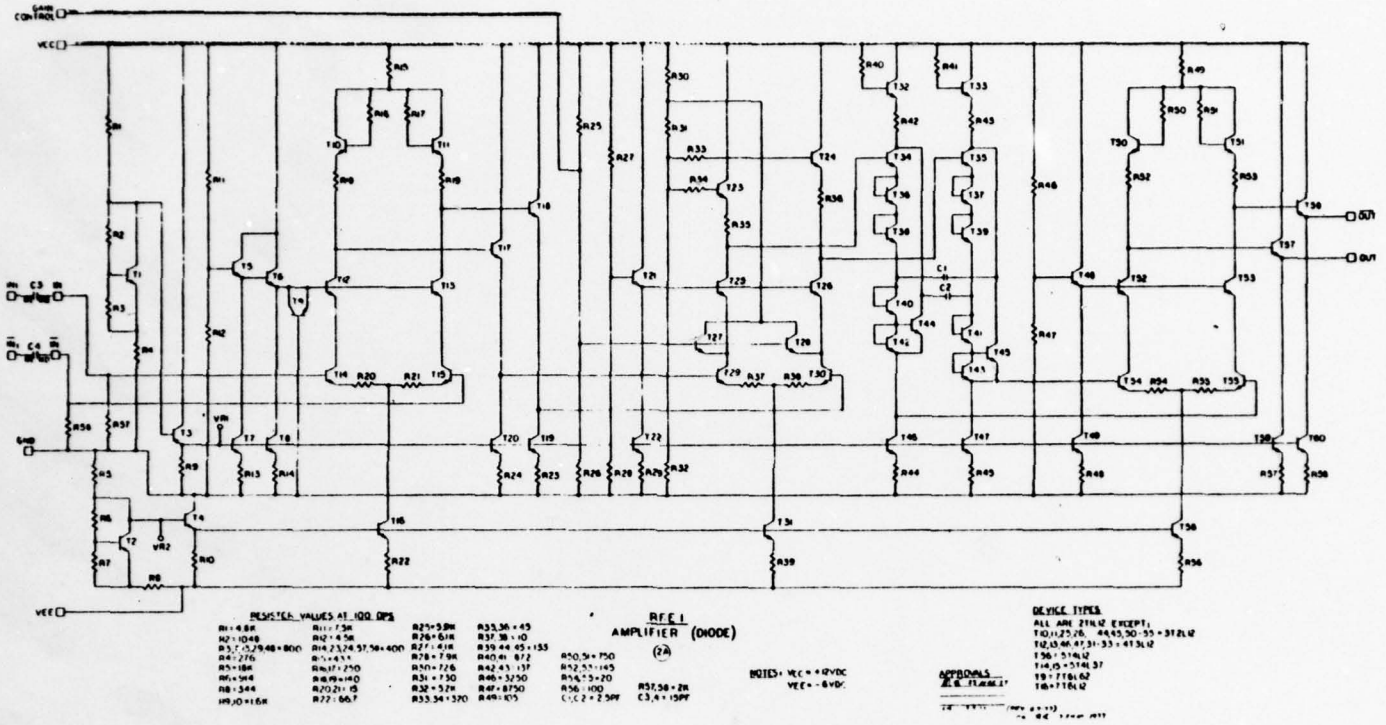


Figure 3-3 Schematic Diagram of RF Amplifier which Utilizes Actively Realized Inductances (T_{10} and T_{11}) for Shunt Peaking Purposes

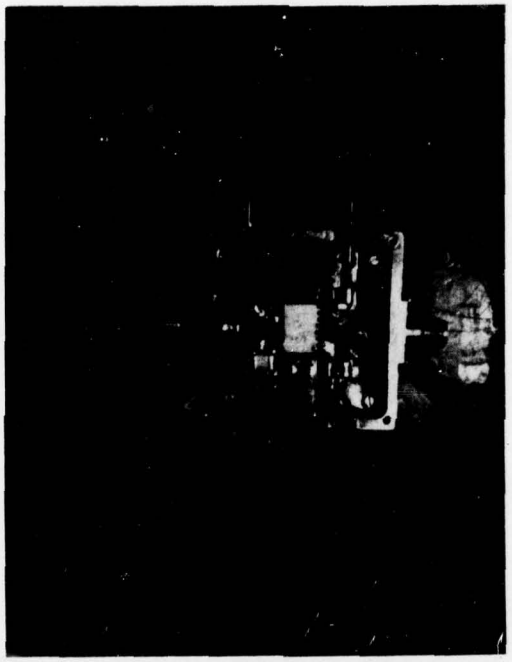
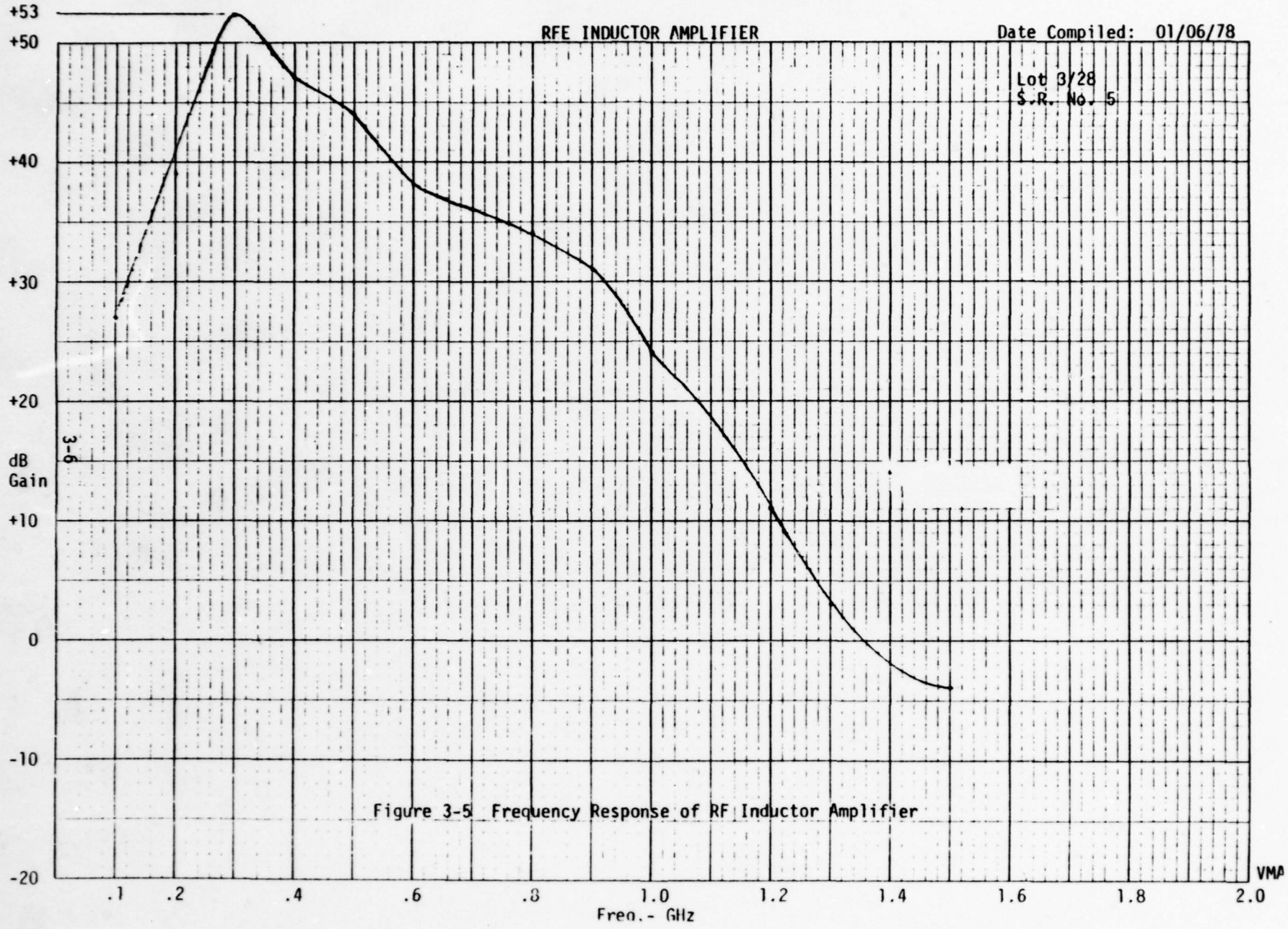


Figure 3-4 Inductor Amplifier Test Fixture



3-6

Figure 3-5 Frequency Response of RF Inductor Amplifier

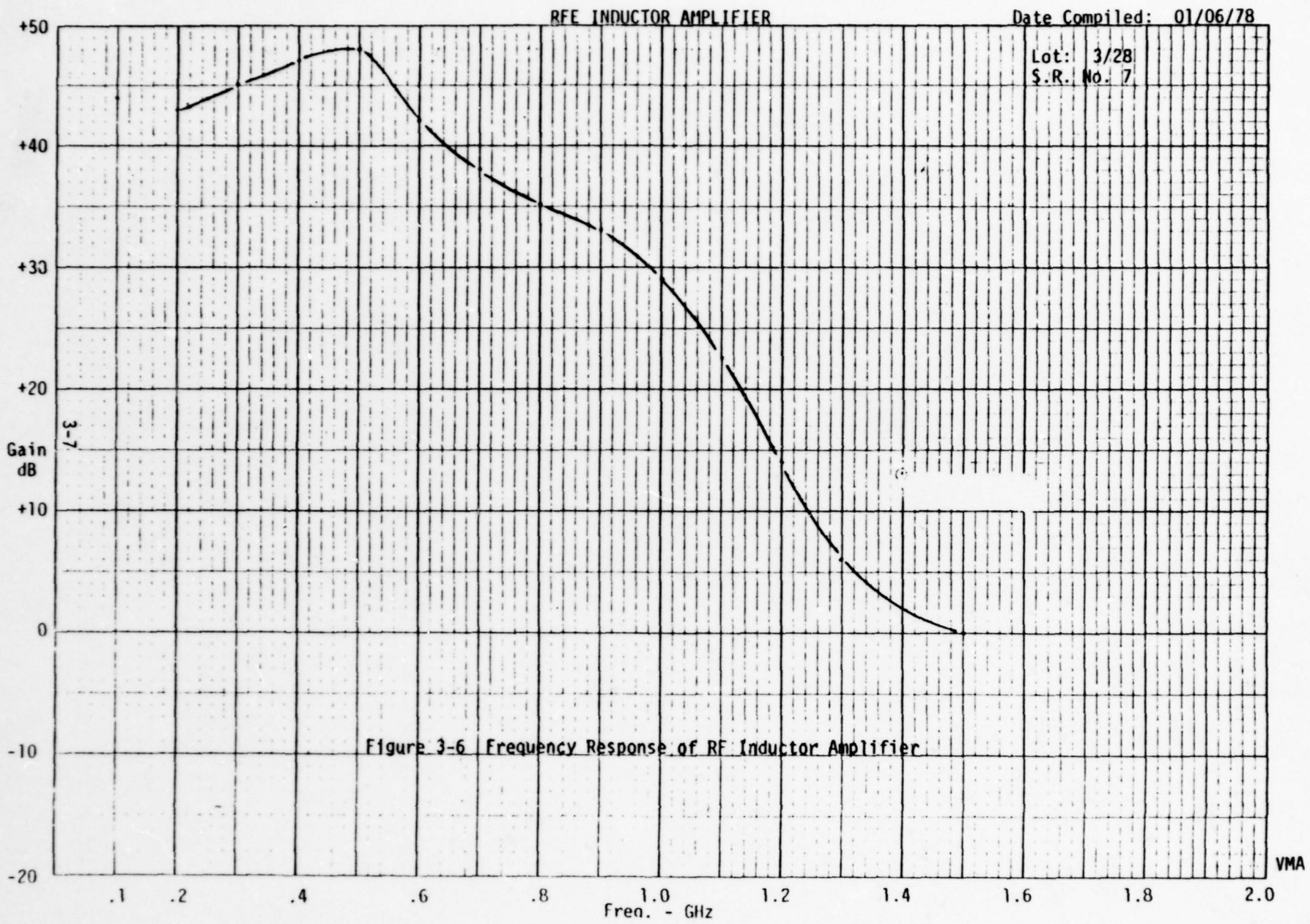


Figure 3-6 Frequency Response of RF Inductor Amplifier

Figure 3-7 Frequency Response of RF Inductor Amplifier

3.1.2 Conclusions

The measured frequency response is deficient and in particular, the upper 3dB corner frequency is virtually a factor of two below anticipated values factored into the design procedure. Moreover, the measured noise figure at 200 MHz is lower than the anticipated value of 1.9dB, but the measured noise figure displays much sharper than expected sensitivity to signal frequency. The reasons for these discrepancies are as follows.

1. First and foremost, the models originally used for all monolithic bipolar junction transistors (MBJTs) are deficient. These models are the classical Ebers-Moll mathematical structures[2] which are incapable of accurately reflecting the distributed nature of the electrical effects of charge transport at very high frequencies. This deficiency is especially predominant when, as in the case of transistors T10 and T11 in the diode amplifier, base pushout is induced by low voltage biasing of the collector-base junction.

   The subsequent use of an advanced MBJT model, developed for the RFLSI program (see Section 3.0 of TASK 1 report), to simulate RF amplifier response confirms the foregoing assertion. In particular, the revised model predicts a nominal bandwidth of 570 MHz.

2. For the inductor amplifier, the peaking evidenced at too low a signal frequency is the direct result of errors made in computing the effective inductance of a metallized pattern. In effect, the inductances are low by a factor of approximately two, due to a variety of on-chip parasitics (see Section 5.2 of TASK 1 report) which were not incorporated in the design procedure.

   Low effective inductance also prevails in the diode amplifier case because of inappropriate biasing. As shown in Section 2.2.2 of the TASK 1 report, inappropriate biasing of a common base stage limits the frequency range over which the impedance seen looking into the emitter is inductive in nature.

3. The use of current sources T16, T31, and T56 is inappropriate at high frequencies because of a substantial capacitive effect induced at the collector (see Section 2.2.2 of TASK 1 report). This capacitance degrades the high frequency common mode response, and it also shifts presumably second order poles to lower frequencies in the differential mode gain characteristic.

4. Base-emitter junction diode strings exude much too slow a frequency response. Alternative configurations (see Section 2.1.6 of TASK 1 report) are substantially more effective.

5. The degraded noise performance is a ramification of the fact that the RF amplifier is direct coupled; i.e., its frequency response extends from zero frequency to the upper 3dB point. Such a wide frequency response has the effect of integrating the noise power spectral density, thereby producing a relatively large "sum" of total output noise[3]. Fortunately, the GPS receiver is configured in such a way that low frequency amplifier performance can be compromised in favor of improved noise characteristics.

3.2 Voltage Controlled Oscillator

A schematic diagram of the voltage controlled oscillator (VCO) is shown in Figure 3-8. Extensive simulations on both the COMPACT and SPICE-2 computer-aided analysis programs have been performed to study loop gain characteristics. Testing has also been accomplished.

3.2.1 Test Results

As exemplified in Figures 3-9 through 3-11 for a variety of VCO samples, the fabricated VCOs oscillate at frequencies in the range of 950 MHz. If properly heat sinked, the circuit oscillates at 1 GHz or even higher frequencies. If the circuit is allowed to heat, the oscillation frequency drops to approximately 930 MHz.

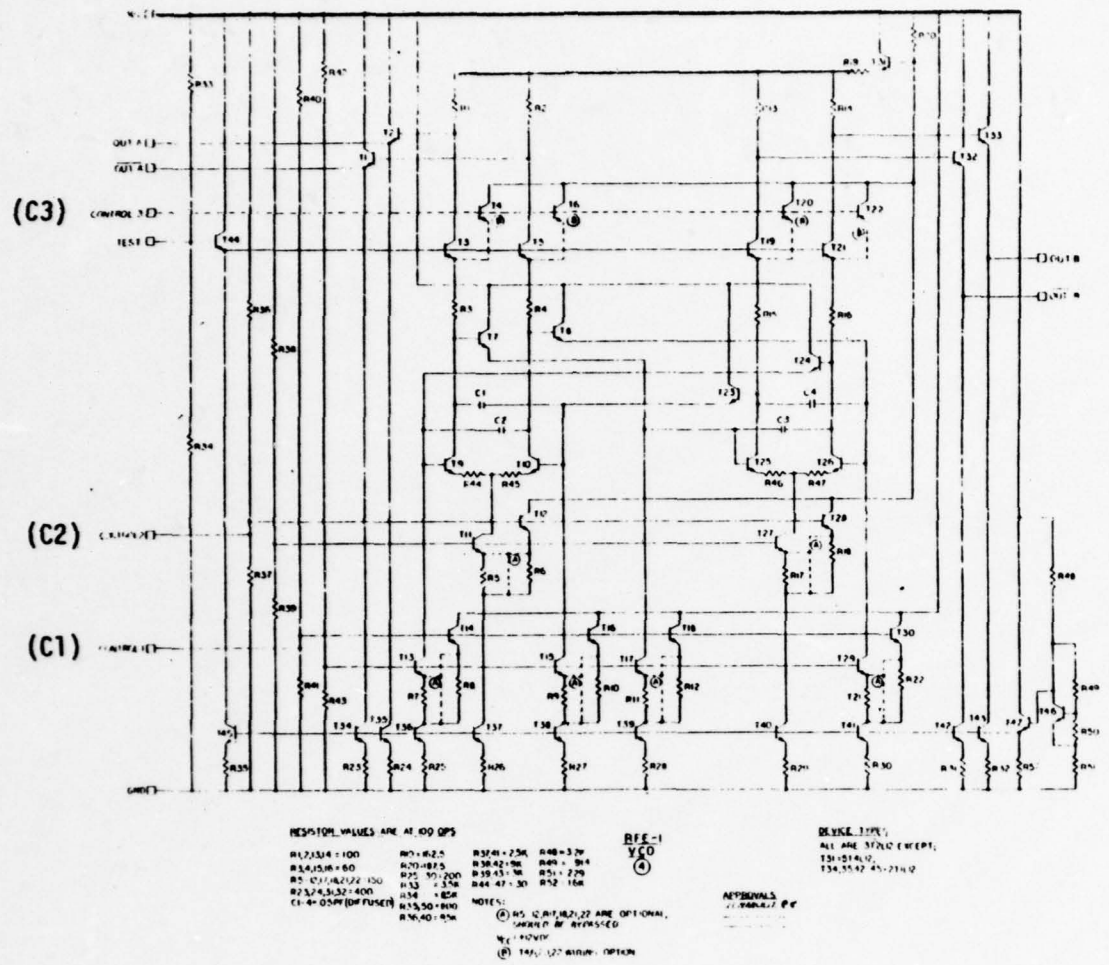


Figure 3-8 Schematic Diagram of VCO

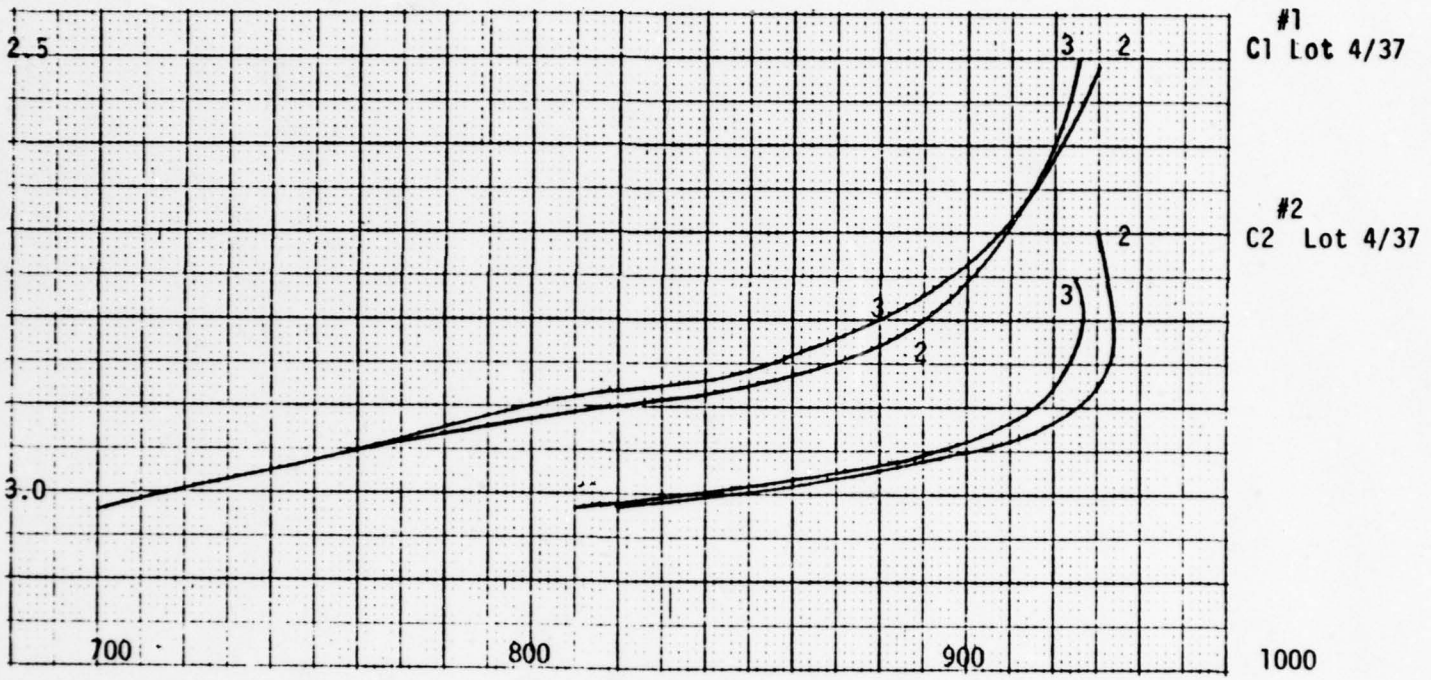


Figure 3-9 Sample VCO Experimental Characteristics

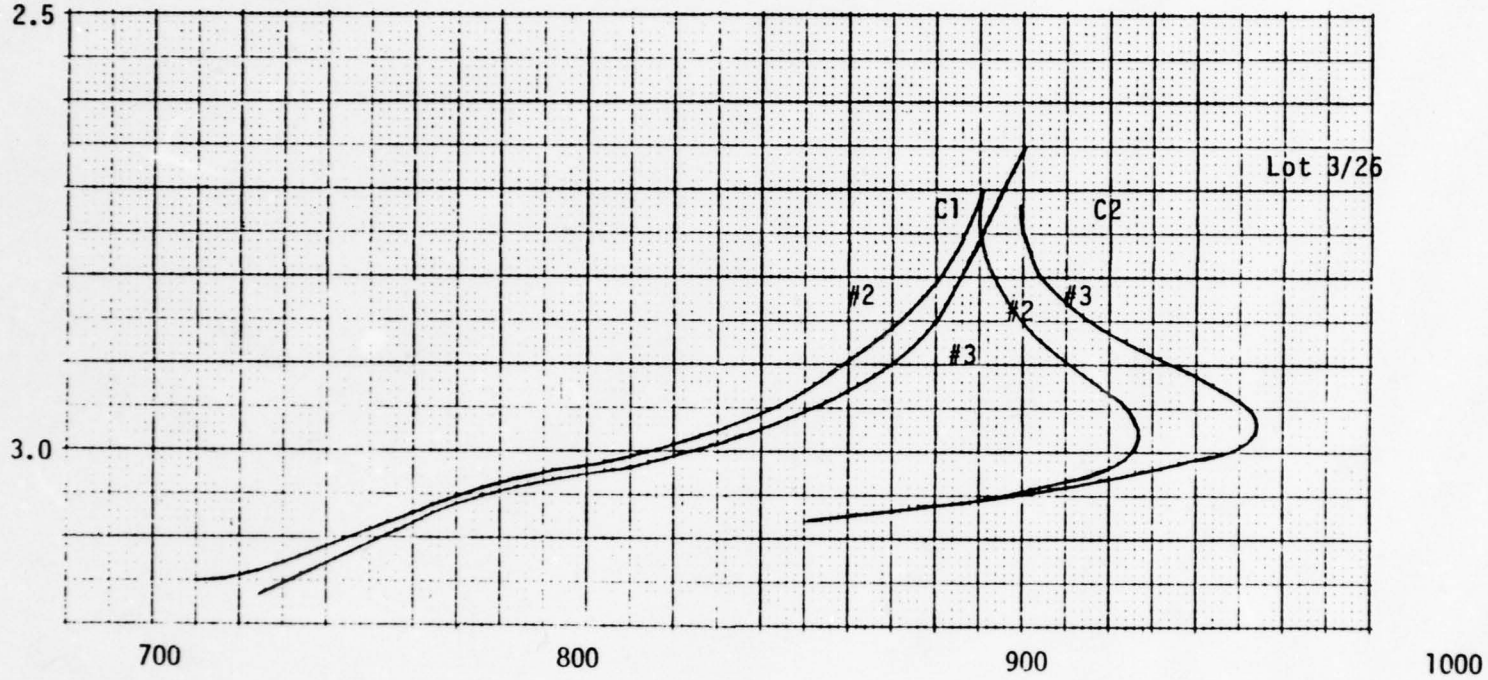


Figure 3-10 Sample VCO Experimental Characteristics

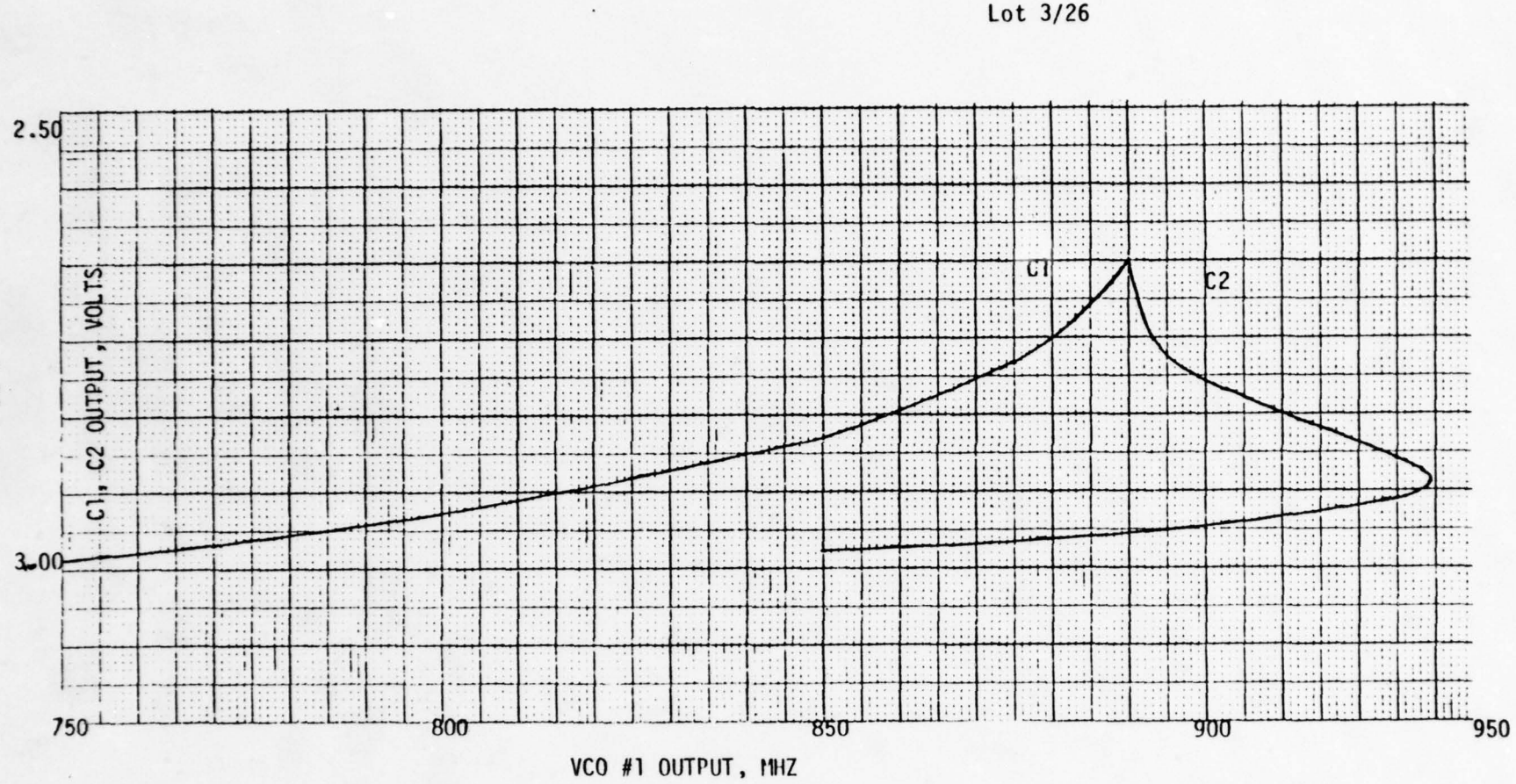


Figure 3-11 Sample VCO Experimental Characteristics

Improved frequency response and thermal characteristics can be achieved through improved biasing (see Section 2.1.7 of TASK 1 report) and by implementing AC coupling via lossless matching circuits at network interstages (see Section 2.3 of TASK 1 report). To this end, the VCO depicted schematically in Figure 3-12 has been extensively analyzed. Two versions of this circuit have been studied. One version is as shown in the diagram, and the other version supplants current sources Q5 and Q6 by resistors. Both versions, and particularly the second, show strong potential for generating oscillation frequencies which match GPS receiver RF requirements. However, the required matching inductors (L_1 through L_4) are too large to practical for monolithic realization, and the tuning varactors require a capacitance-voltage variation that appears to exude too broad a range for realiable integrated circuit design.

At this juncture, the most promising VCO appears to be one which exploits frequency doubling techniques, as discussed in Section 7.2.3 of the TASK 1 report. Yet another alternative is one which makes use of the negative resistance established at the base of a transistor by interaction of intrinsic transit time delays and the electrical properties of a tuned collector load[4]-[5].

3.3 Phase Logic Demodulator (PLD)

3.3.1 Schematic and Test Results

The schematic diagram of the phase logic demodulator is shown in Figure 3-13. Sample circuits have been probed with the "micromanipulator" probes. The percentage of circuits showing the proper dc levels is small. However, the layout of the circuit has been checked, no errors are apparent. The cause of the dc offset problems in the PLD are under investigation. Additional measurements and computer simulations are presently being performed to pinpoint the difficulty.

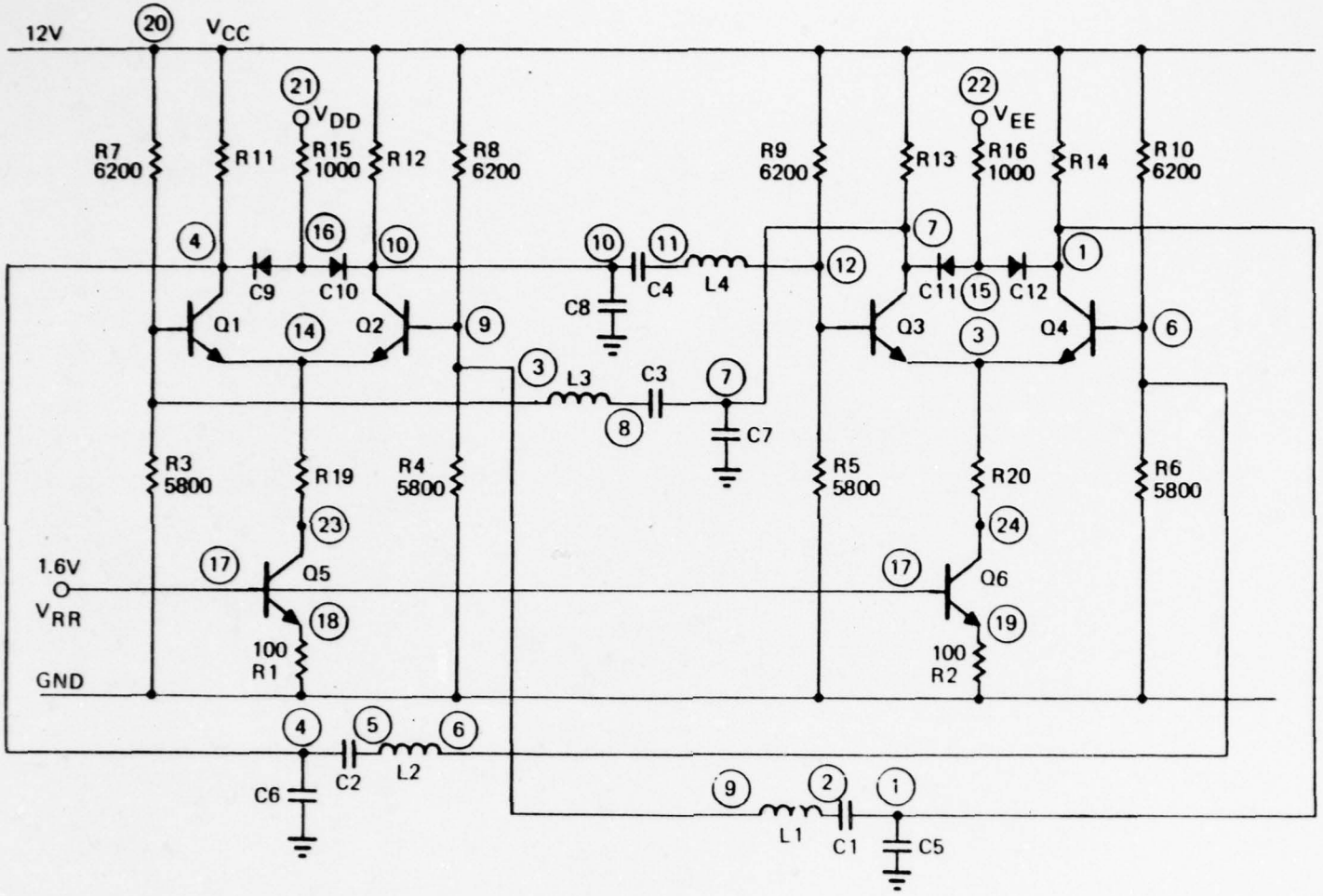


Figure 3-12 Simplified Alternative VCO Schematic Diagram

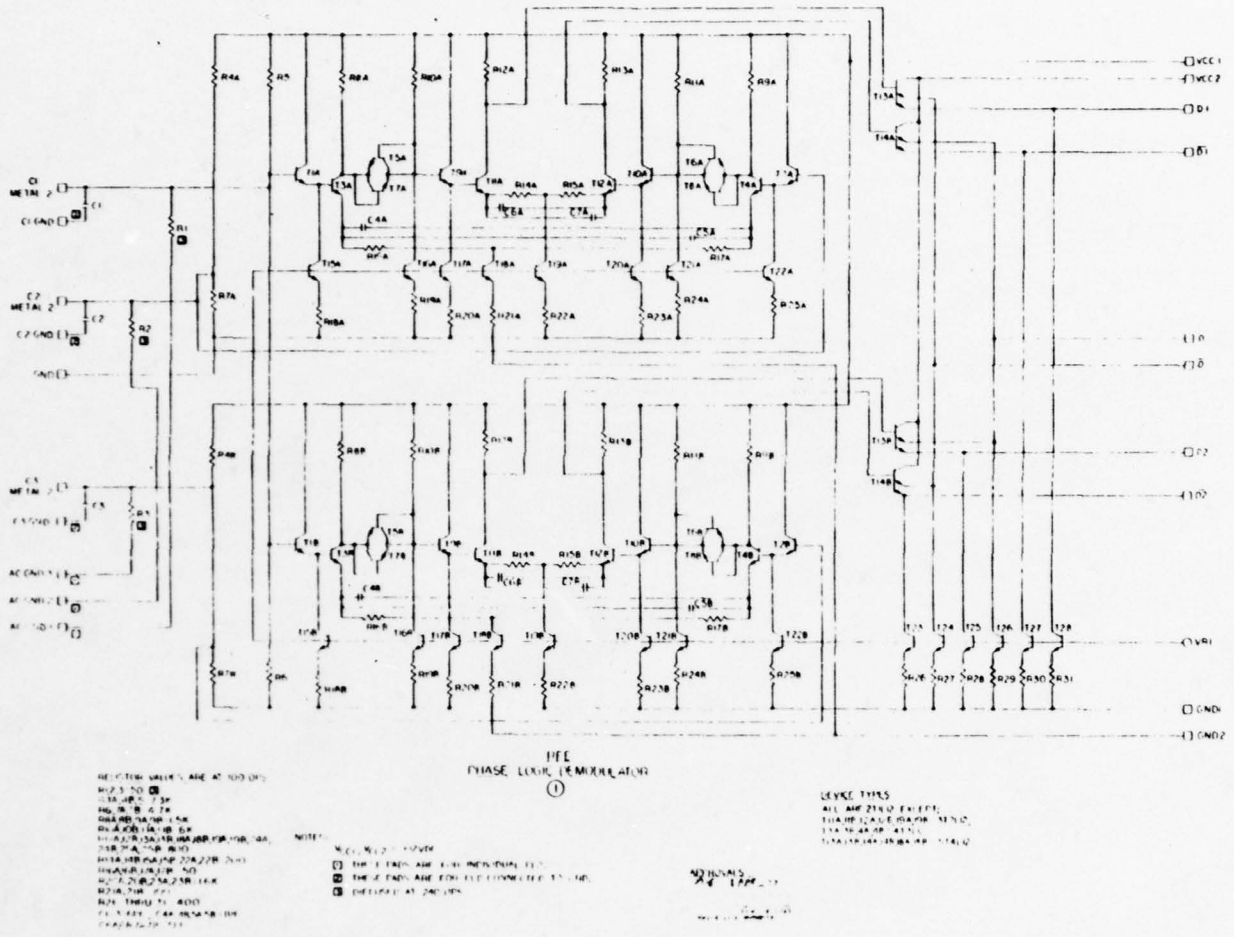


Figure 3-13 RFE Phase Logic Demodulator

3.3.2 Costas Loop/Phase Detector

Because of the foregoing PLD difficulties and an apparent lack of control that can be exerted on both loop and noise bandwidths, the Costas demodulator, which is mathematically equivalent to the PLD, is a viable design alternative. The potential applications and an analysis of the Costas loop are provided in Section 7.0 of the TASK 1 report.

The block diagram, performance goals, measured performance, and photograph of the fabricated Costas demodulator are shown in Figure 3-14. It is important to record that the phase detector, whose schematic diagram appears in Figure 3-15, performed extremely well over the frequency range of 0-to-4 GHz. When driven by 40mV peak-to-peak amplitude signals, its differential gain is 24.6dB, its common mode gain is 32dB and it possesses a dynamic range of 41dB. Dynamic range is defined herewith as the ratio of the peak-to-peak amplitude of the output signal to the quiescent offset amplitude.

3.4 Analog Multiplier Tests

It should be noted that the phase detector of Figure 3-15 is indeed an analog multiplier. As pointed out during the course of analyzing analog multipliers in Section 6.0 of the TASK 1 report, the operation of the GPS mixer circuits constitutes a critical system function. In particular, the idealized mixer is one in which the output is a linear function of the product of a pair of input signals. In Figures 3-15 and 3-16, let the two input signals be written

$$V_1 = A \sin\omega_1 t$$

and

$$V_2 = B \sin\omega_2 t.$$

Then the idealized output signal is

$$V_0 = KV_1V_2 = KAB \sin(\omega_1 t) \sin(\omega_2 t),$$

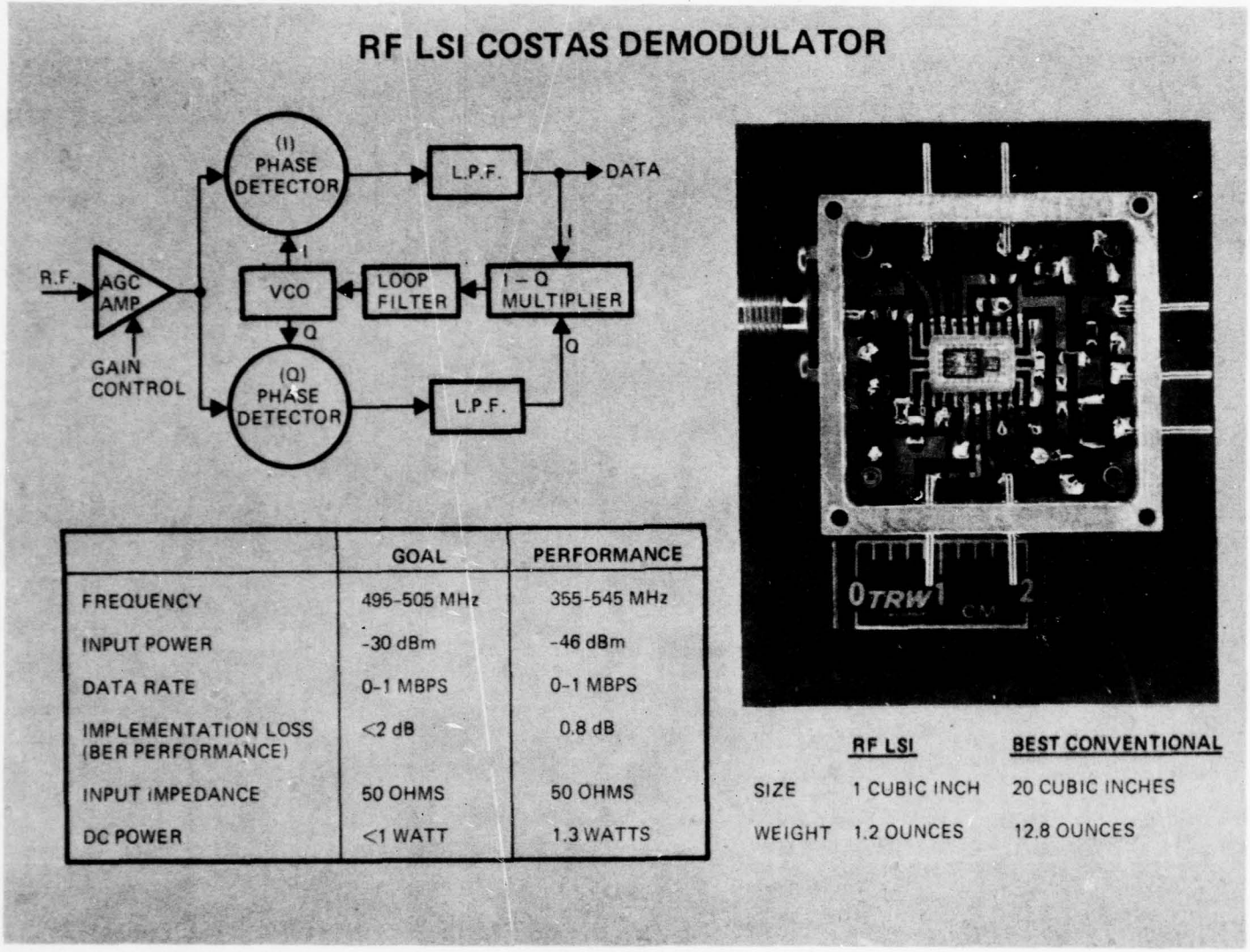
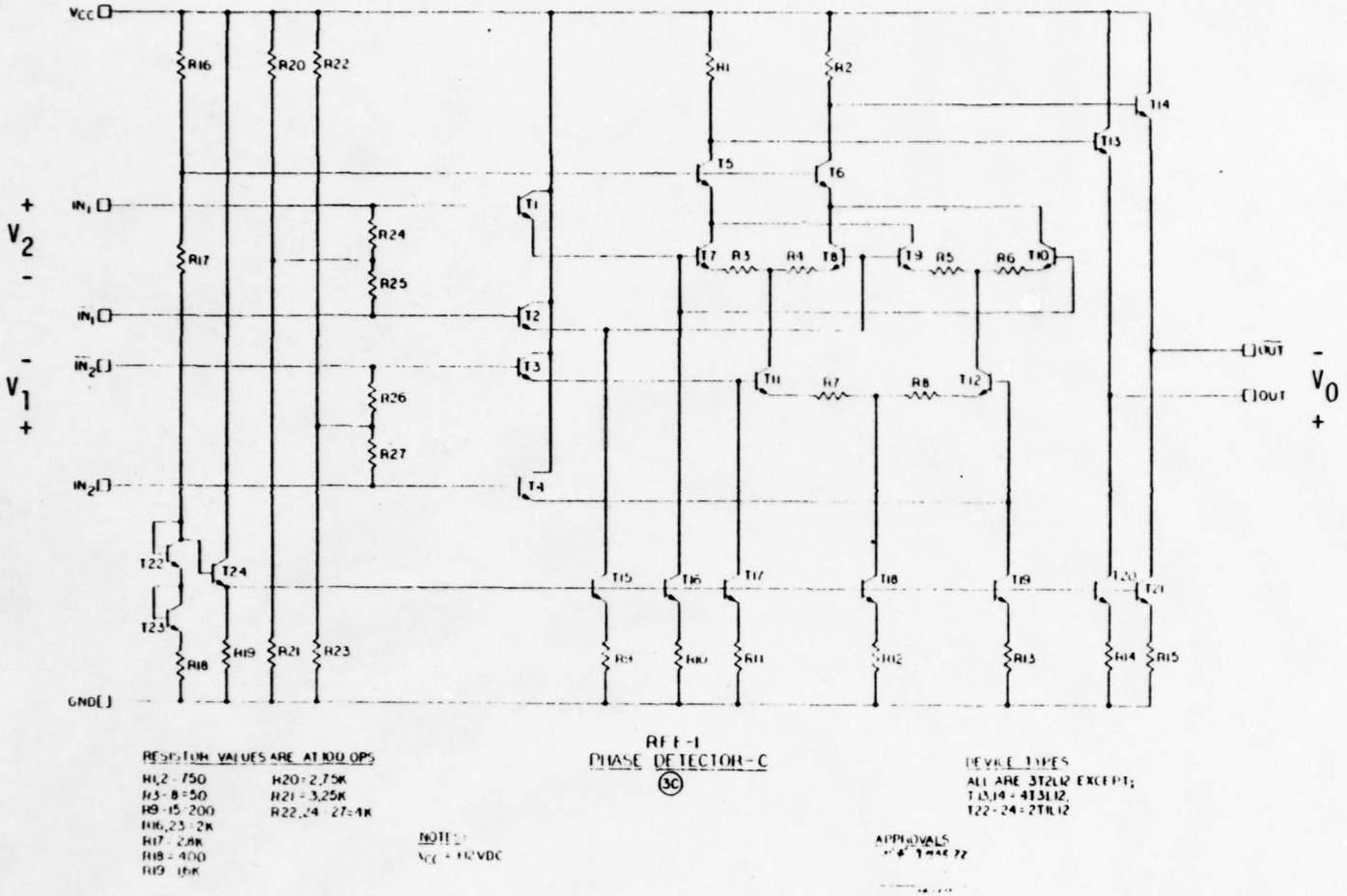


Figure 3-14 RF LSI Costas Demodulator



RESISTOR VALUES ARE AT 100 OPS

R1,2 - 750
R3 - 8 = 50
R9 - 15 = 200
R16,23 = 2K
R17 = 2.8K
R18 = 400
R19 = 6K
R20 = 2.75K
R21 = 3.25K
R22,24 - 27 = 4K

RFE-1
PHASE DETECTOR-C
(3C)

DEVICE TYPES
ALL ARE 3T2L12 EXCEPT;
T13,14 = 4T3L12,
T22 - 24 = 2T1L12

NOTES:
VCC = +10VDC

APPROVALS

Figure 3-15 RF LSI Phase Detector

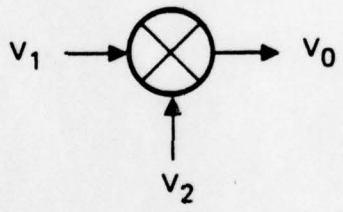


Figure 3-16 Symbolic Illustration of an Analog Signal Multiplier

which clearly contains only the sum and difference frequencies, $(\omega_1 + \omega_2)$ and $(\omega_1 - \omega_2)$. Frequencies other than these sum and difference frequencies in a practical mixer realization are termed spurious frequencies. The quality of a practical mixer is in one-to-one correspondence to its ability to suppress spurious frequencies. Moreover, an idealized mixer is able to sustain constant conversion gain, K, independent of ω_1, ω_2, and the sum and difference frequencies. Accordingly, the analytical work performed on contract was supplemented by considerable experimental work aimed toward understanding the requirements of a mixer that is optimal in the sense of closely replicating idealized performance.

3.4.1 Conversion Gain

The amplitudes of V_1 and V_2 are fixed at -30dBm which preclude overdrive of all transistors, and the frequencies of V_1 and V_2, f_1 and f_2, respectively, are varied from zero to 1 GHz. The amplitude of the output signal component at the difference frequencies, $\pm(f_1 - f_2)$ is recorded and divided by the product of the signal amplitudes of V_1 and V_2. This "gain" is symbolized as K, and plots of f_1 versus f_2 for constant K_1 are generated, as shown in Figure 3-17. Observe that for fixed input amplitudes the curves provide information as to the output signal amplitude generated for given input signal frequencies.

3.4.2 Spurious Frequencies

The ramifications of signal overdrive are depicted in Figures 3-18 and 3-19. As anticipated, spurious frequency generation becomes troublesome for progressively increasing input signal amplitudes. A close inspection of these experimental results in light of analyses documented in Section 6.0 of the TASK 1 report infers that input signal amplitudes must be kept below approximately $2V_T$ (52mV at room temperature) if amplitudes of spur signals are to be inconsequential.

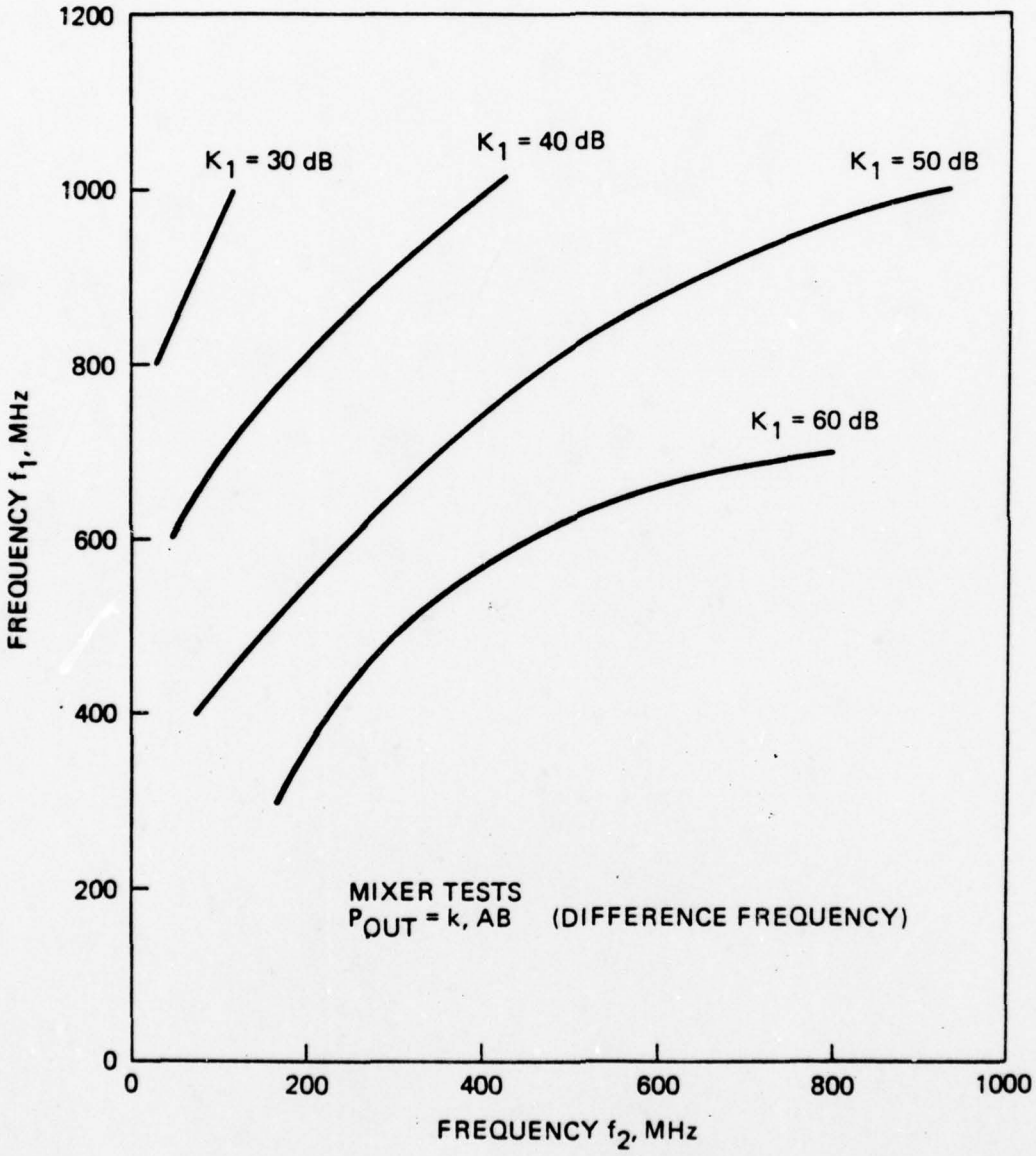
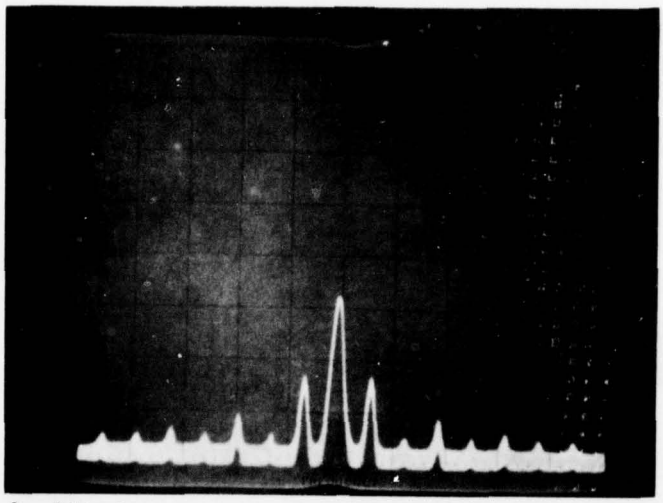
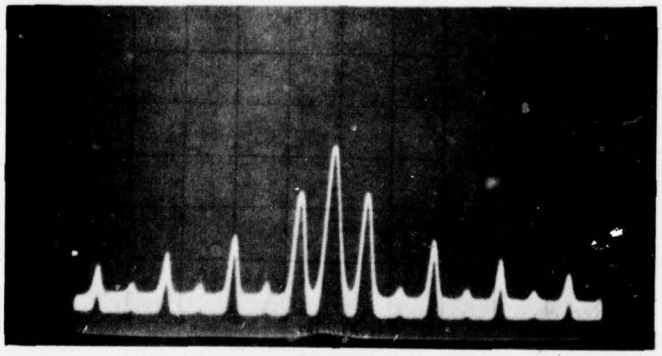


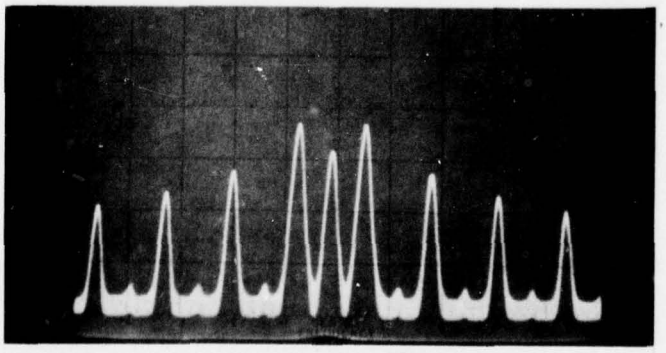
Figure 3-17 Contours of Constant Conversion Gain



Amplitude of V1 = 15mV, PP

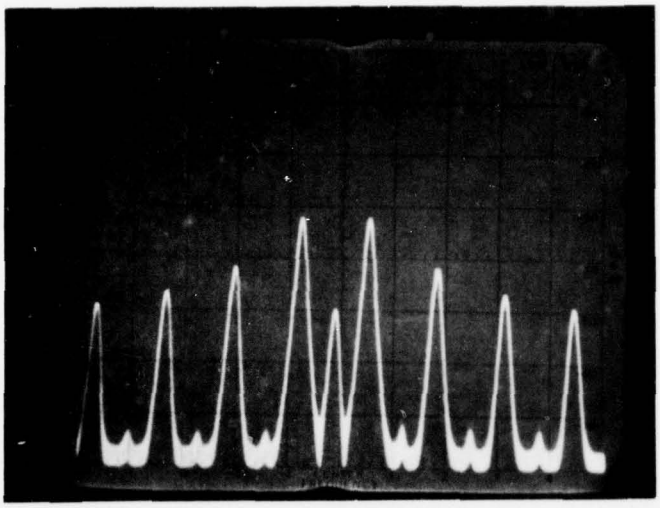


V1 = 40mV, PP

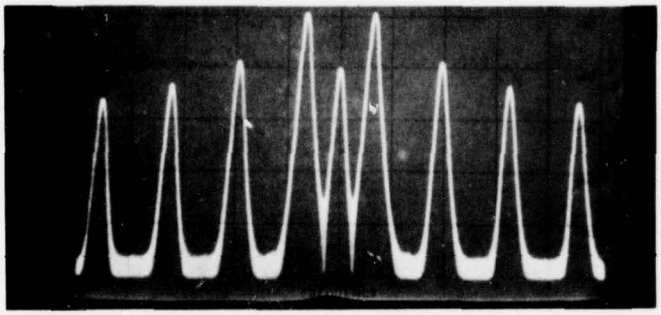


V1 = 200mV, PP

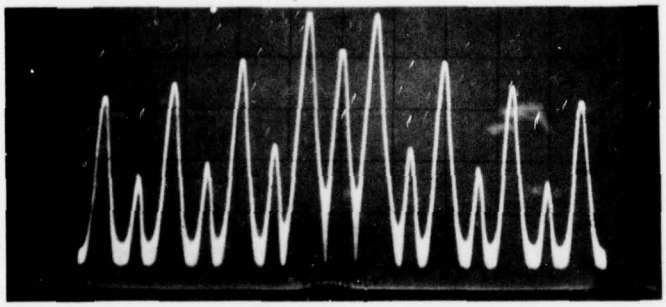
Figure 3-18 Output Spectrum Response to Modulating Input Applied as V_1 in Figure 3-15



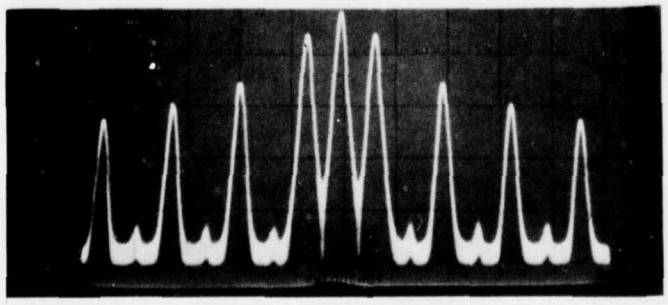
V1 = 600mV, PP



V1 = 4V, PP

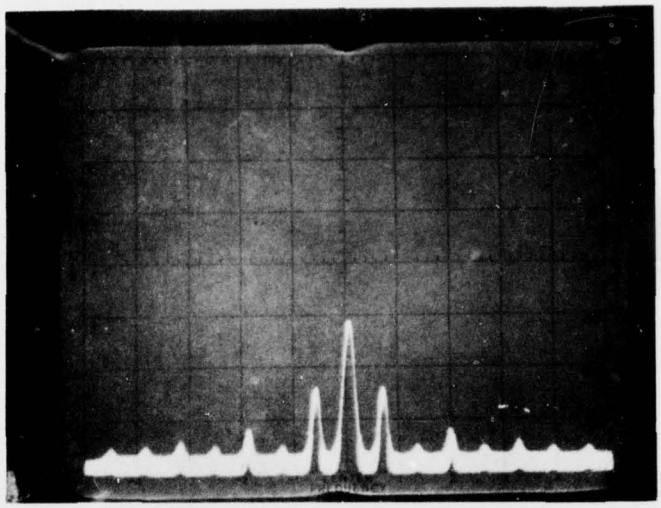


V1 = 6V, PP

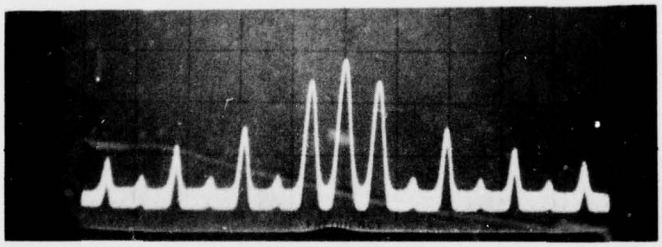


V1 = 7.5V, PP

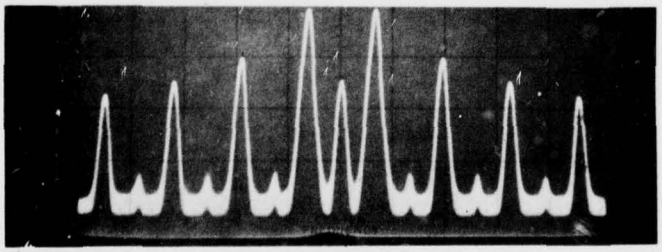
Figure 3-18 (concluded)



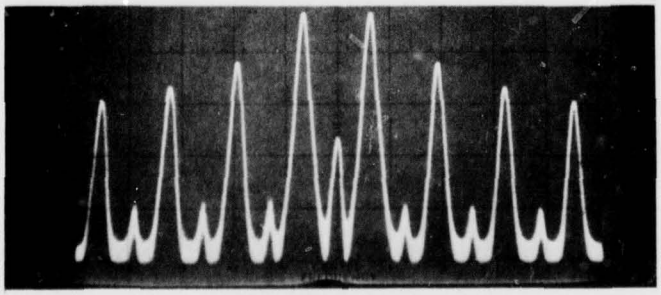
Amplitude of V2 = 15mV, PP



V2 = 40mV, PP

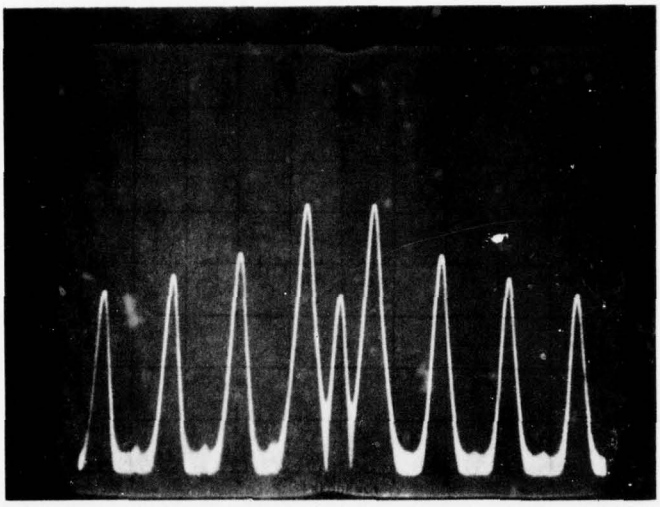


V2 = 200mV, PP

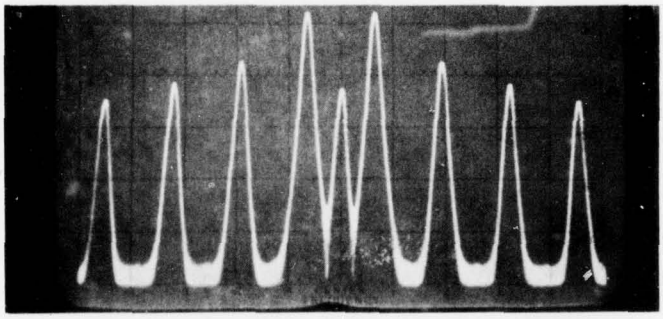


V2 = 400mV, PP

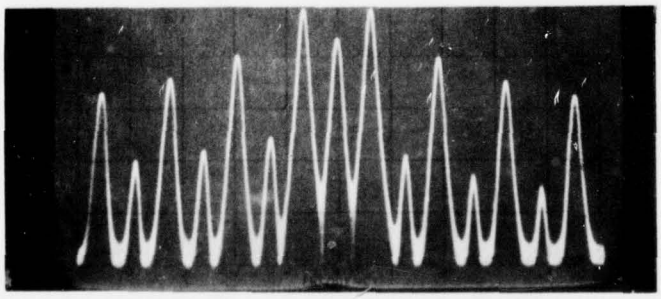
Figure 3-19 Output Spectrum Response to Modulating Input Applied as V2 in Figure 3-15



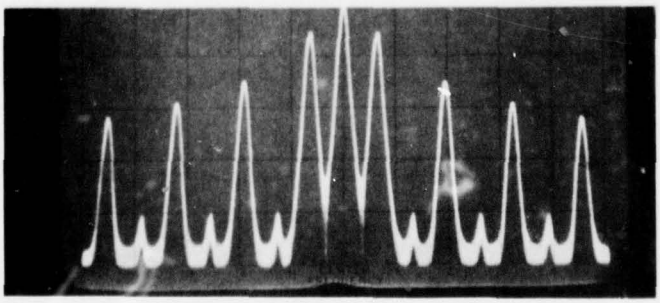
V2 = 600mV, PP



V2 = 4V, PP



V2 = 5.4V, PP



V2 = 7V, PP

Figure 3-19 (concluded)

4.0 GPS CHIP REALIZATION

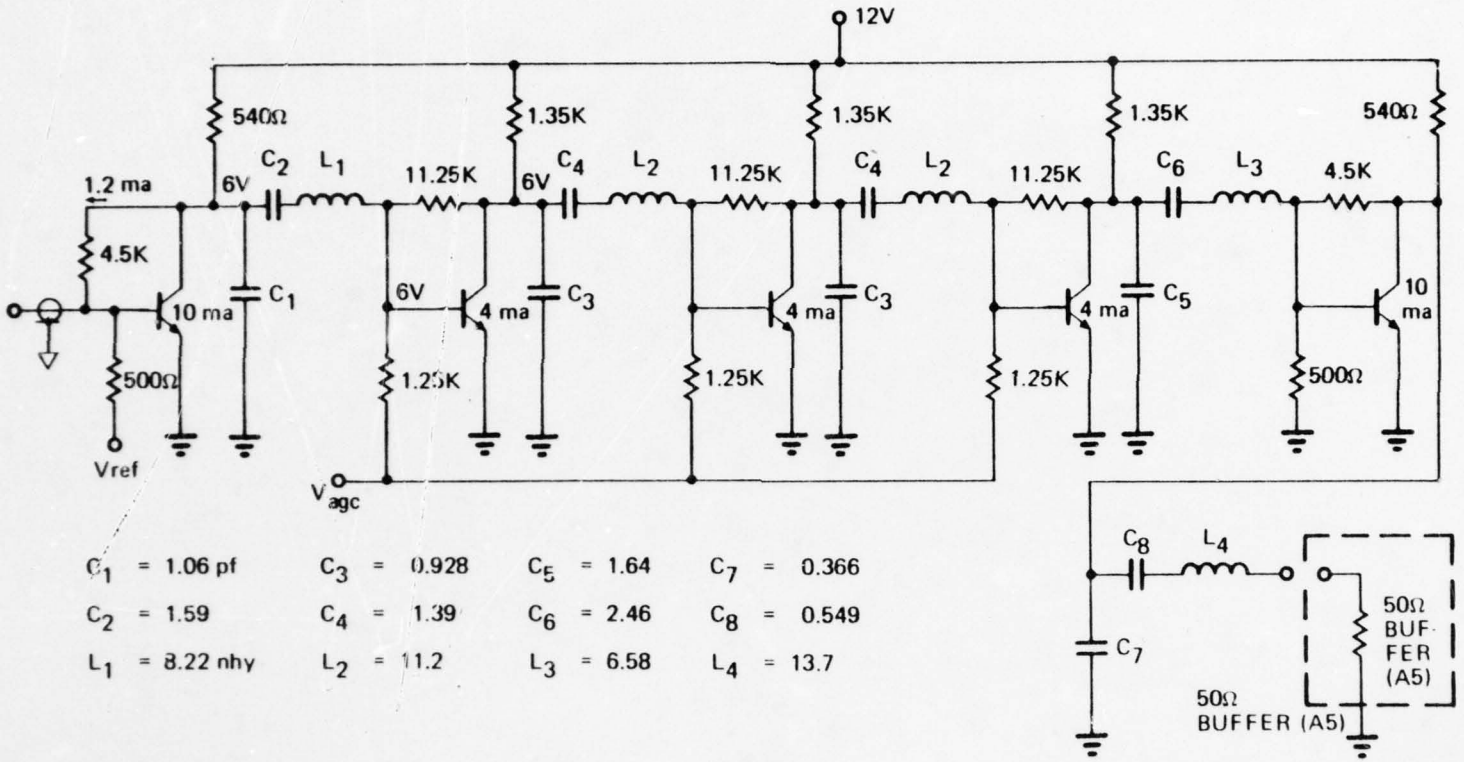
The finalized form of the system schematic diagram for the GPS test chip is shown in Figure 2-6 of this report. The circuitry implicit in the chip exploits the basic research and development accomplished in TASK 1. The test chip is designed to be compatible with the GPS receiver development program of the United States Navy.

4.1 RF Amplifier (A1)

The schematic diagram of the RF amplifier is depicted in Figure 4-1. The amplifier is a cascade of five voltage feedback amplifiers which utilizes lossless networks for interstage matching networks. Automatic gain control (AGC) is achieved by through bias current variation in the center three stages. Provisions are made at the input stage to optimize noise figure through variation of bias current by adjusting applied voltage V_{REF}. Table 4-1 defines the pertinent electrical specifications.

4.2 Buffer Amplifiers (A5)

Two buffer amplifiers, symbolized as A5 in the system schematic of Figure 2-6, are utilized in the GPS test chip. One appears between the RF amplifier and mixer M1, and the other is used as an interface between the local oscillator (LO) output and a second input to mixer M1. In each case, the buffer performs the required function of supplying differential signal drive to the mixer. The buffer amplifier, whose schematic diagram appears in Figure 4-2, consists of a differential amplifier stage with one input ground, lossless matching network at the input, and a pair of output lossless networks. The output LC networks are used to present loads to the differential stage which ensure that the two output signal powers are identical. In other words, these networks compensate for high frequency current gain mismatch between the two transistors used in the differential stage.



C_1	= 1.06 pf	C_3	= 0.928	C_5	= 1.64	C_7	= 0.366
C_2	= 1.59	C_4	= 1.39	C_6	= 2.46	C_8	= 0.549
L_1	= 8.22 nhy	L_2	= 11.2	L_3	= 6.58	L_4	= 13.7

Figure 4-1 Schematic Diagram of RF Amplifier (A1)

TABLE 4-1 RF AMPLIFIER (A_1) SPECIFICATIONS

FREQUENCY:	1575 MHz $\pm$ 20 MHz (1dB B.W.)
GAIN:	+15 to +30dB
AGC RANGE:	15dB
INPUT LEVELS:	-76dBm to -40dBm
OUTPUT LEVELS:	-46dBm to -25dBm (1dB compression $\geq$ -15dBm)
NOISE FIGURE:	3dB (at low gain)
INPUT IMPEDANCE:	50 ohms (single ended) VSWR $\leq$ 2:1
OUTPUT IMPEDANCE:	Compatible with Mixer M_1 input
DC POWER:	$\leq$ 600 mW

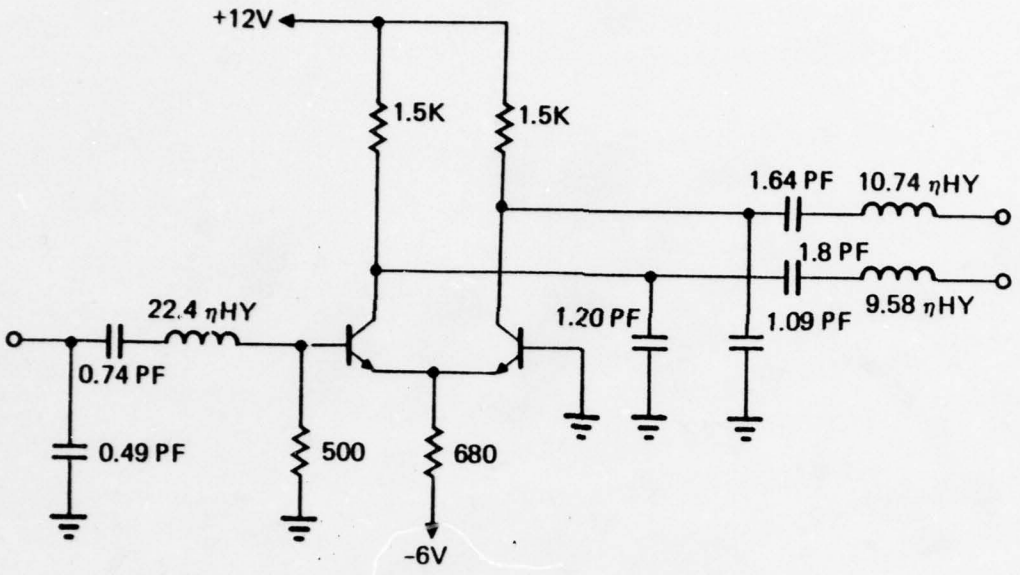


Figure 4-2 Schematic Diagram of Buffer Amplifier (A5)

4.3 IF Amplifier (A2)

Figure 4-3 is the schematic diagram of the IF amplifier (A2). This circuit is a two-stage differential configuration with single-ended emitter follower output and thermally compensated input. The two input capacitors obviate the need for DC level shifting at the mixer M1 - amplifier A2 interface. A manual gain control (MGC) is included to set the composite gain of mixer M1 - amplifier A2 to approximately 13dB. To preclude the need for further gain adjustments due to thermally-induced shifts in critical transistor parameters, a diode-connected transistor (D) is inserted as shown. Table 4-2 defines the design specifications of the IF amplifier.

4.4 Mixer (M1)

The three input mixer, labeled as M1a and M1b in Figure 2-6, is offered schematically in Figure 4-4. Its features and advantages over two separate mixers are discussed in Section 2.2 of this report. Table 4-3 lists all cognate specifications.

4.5 Detector and τ_{REF} Multiplier (D and M2)

The combined schematic diagram of the detector and τ_{REF} multiplier is given in Figure 4-5. The input stage is composed of differential pair T5-T6 in cascode with transistors T7-T8. The differential signal developed across the 400 ohm loads in the T7-T8 cascode is applied to the bases of differential pair T9-T10 which, in turn, are in cascode with transistors T11-T12.

When the collector current of T11 or T12 increases above its quiescent operating level, the excess current flows through the emitter of T15 or T16. The combined collector current of T15 and T16 is the detected signal. Transistors T13 and T14 operate as diodes which limit positive voltage excursions at collectors of T11 and T12.

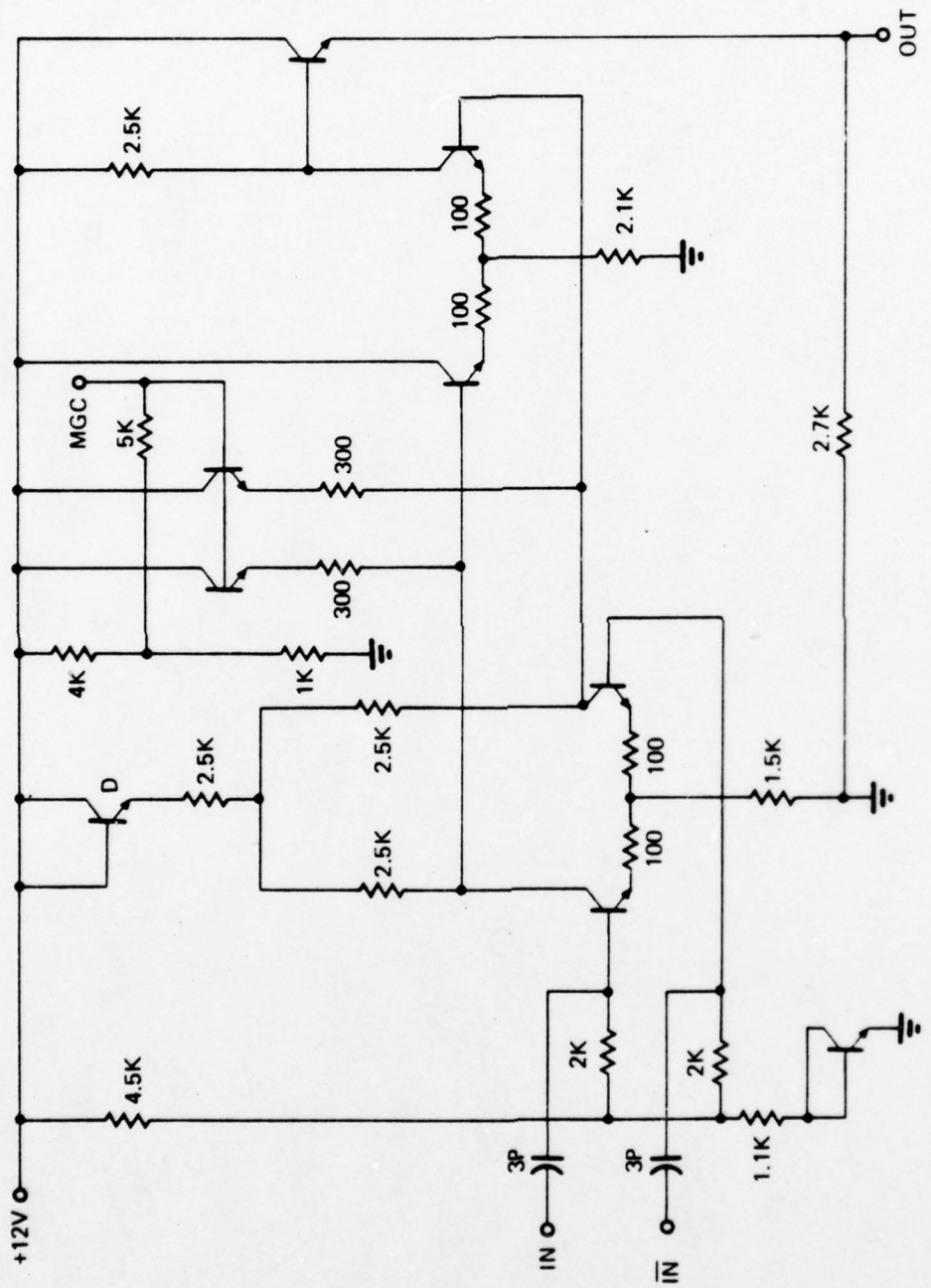


Figure 4-3 IF Amplifier Schematic Diagram

TABLE 4-2 IF AMPLIFIER (A_2) SPECIFICATIONS

FREQUENCY:	143.22 MHz $\pm$ 20 MHz (1dB B.W.)
GAIN:	23dB (with zero MGC adjustment)
INPUT LEVEL:	-56dBm to -35dBm (with zero MGC adjustment)
OUTPUT LEVEL:	-33dBm to -12dBm (1dB gain compression point $\geq$ 0dBm)
INPUT:	Balanced, Compatible with Mixer M_1 Output
OUTPUT:	50 ohms, Single Ended

TABLE 4-3 MIXER M_1 SPECIFICATIONS

INPUT FROM RFAMP/BUFFER:	1575 MHz ± 20 MHz (1dB B.W.) -46dBm to -25dBm Balanced, Compatible with Amplifier A_1 Output
INPUT FROM LO BUFFER:	1432.2 MHz ± 20 MHz (1dB B.W.) -20dBm (constant)
INPUT FROM CODE RECLOCK REGISTER:	Code at 1.023 MBPS or 10.23 MBPS
OUTPUT:	143.22 MHz ± 20 MHz (1dB B.W.) -56dBm to -35dBm (estimated) Balanced, Compatible with Amplifier A_2 Input

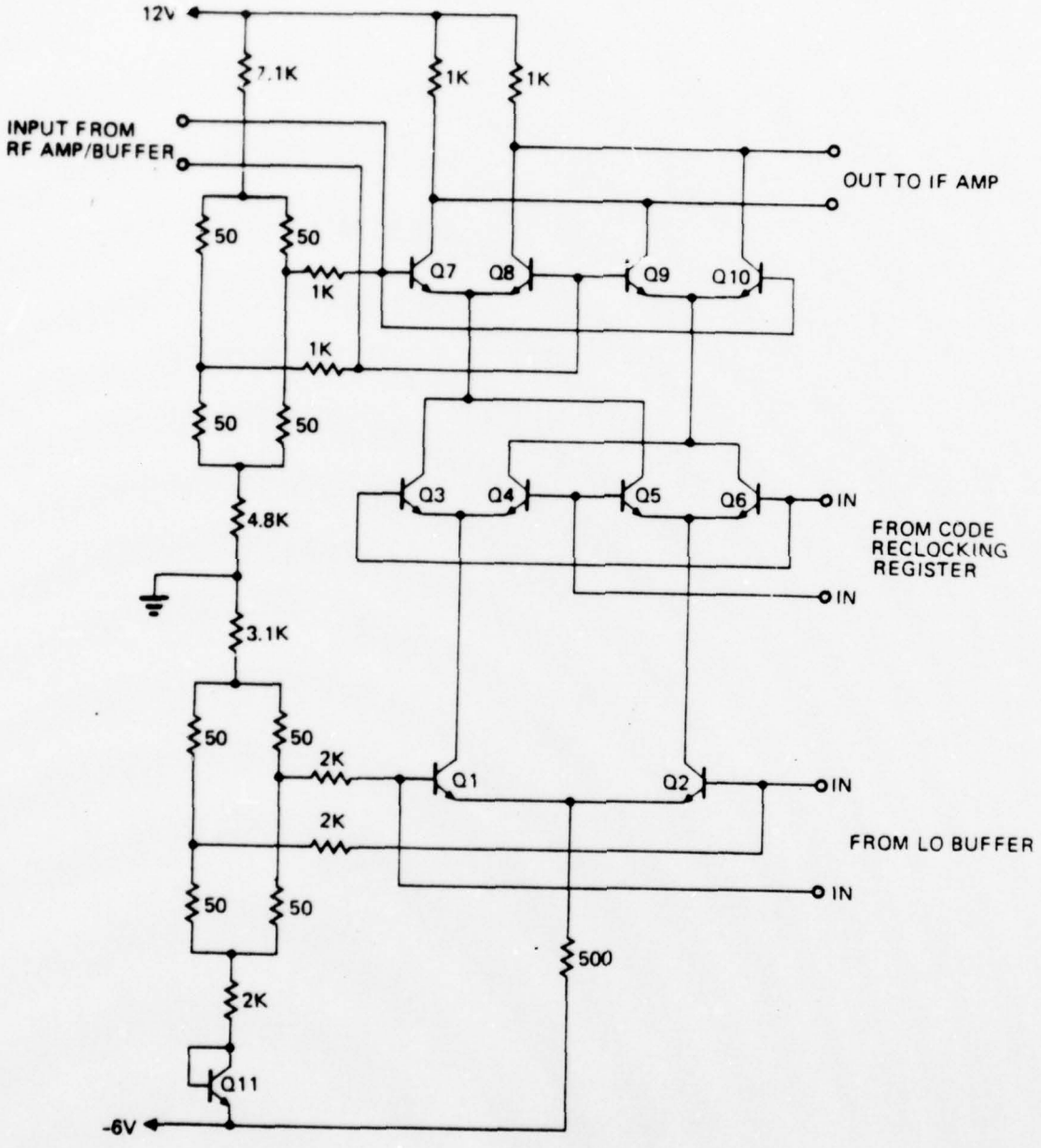


Figure 4-4 Schematic Diagram of Three-Input Mixer (M1a and M1b)

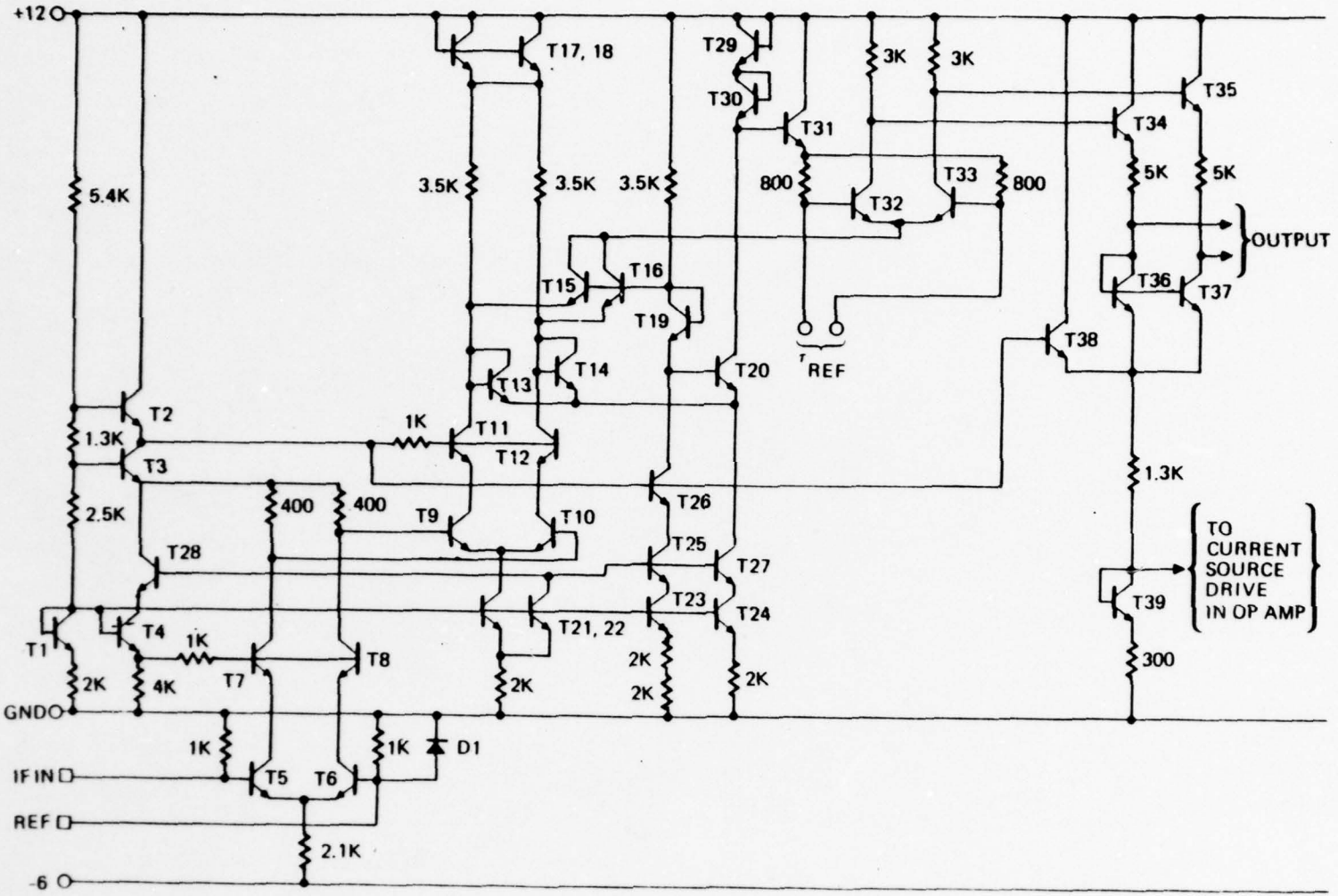


Figure 4-5 Detector and τ_{REF} Multiplier Schematic Diagram

The biasing network consisting of T17, T18, T19, T20, and the 3.5K resistor to the collector of T19 sets the voltages at both the bases of T15-T16 and emitters of T13-T14 to the correct levels. Transistors T17, T18, T19, T20 are scaled to 25 times the emitter area of T13, T14, T15, and T16 to reduce the quiescent bias current into the detector output (T15, T16). The current sources (T21, T22, T23) operate at an exact 2:1 ratio; T25, T26, T27, T28 compensate for various base currents so that the quiescent currents flowing in all three 3.5K resistors are identical and independent of transistor β.

The "τ_{REF} multiplier" is the differential pair T32-T33. This circuit switches the detector output current into one of two load resistors, depending on whether τ_{REF} is positive or negative. The output voltage across the 3K load resistors is the level shifted and converted to a single-ended output signal at the collector of T37.

4.6 Operational Amplifier and Comparator (A3 and A4)

Both the operational amplifier and the comparator utilize the basic gain cell depicted in Figure 4-6. The transconductance of the differential quad formed by T7 through T10 can be very large, depending on the source impedance seen at the basis of T7 and T8. Note that the DC input resistance of the quad, looking into these bases is negative. A first order estimate of this resistance, neglecting terms in beta and also neglecting the collector output conductance gives a transconductance approaching infinity as the effective source resistance at the bases of T7 and T8 approaches $-2(r_e + r_b/\beta_o)$ where r_e and r_b respectively represent emitter and base resistances, and β_o is the low frequency common emitter short circuit current gain. This source resistance is approximated by the impedance presented by the emitters of T3 and T4. Use of the cascode transistors T5 and T6 ensures that T7 through T10 all dissipate the same power, and therefore operate at the same temperature without cascoding, the circuit can become unstable and latch if T7 and T8 operate significantly hotter than T9 and T10.

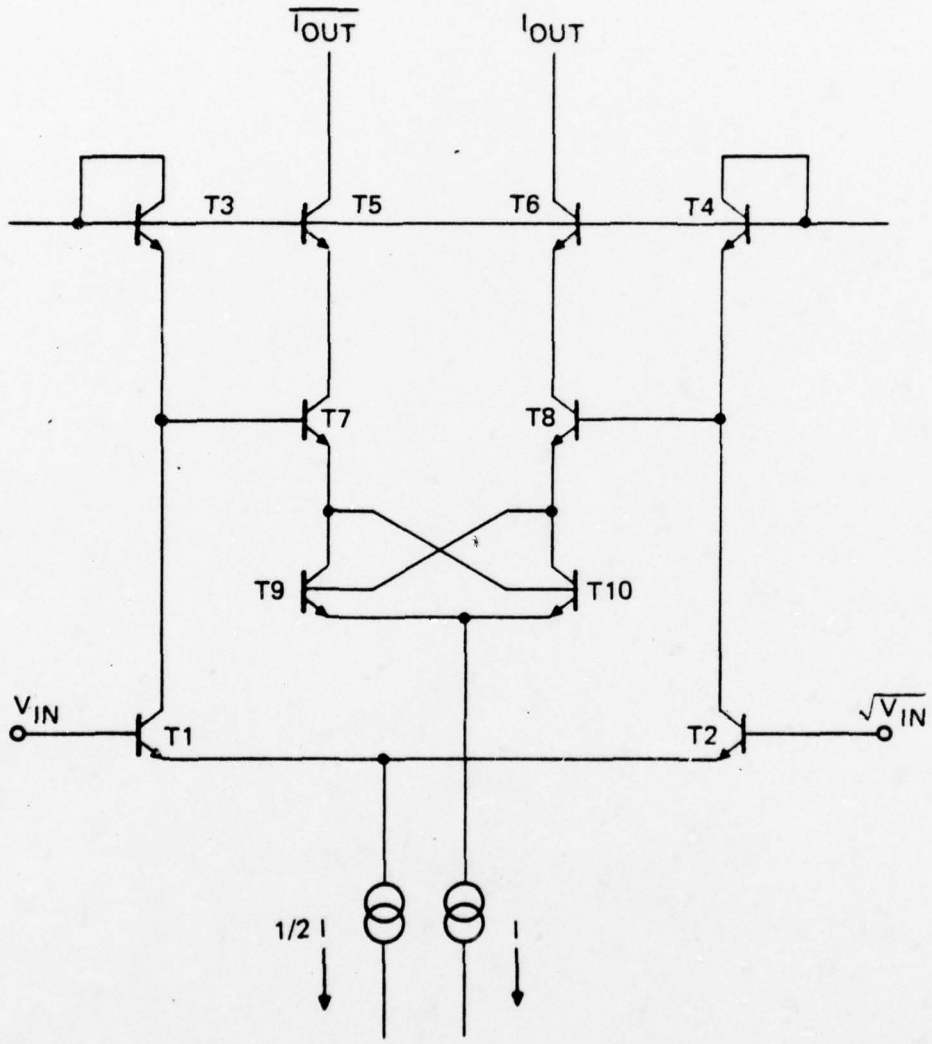


Figure 4-6 Basic Gain Cell for Operational Amplifier and Comparator

4.6.1 Operational Amplifier

The pertinent schematic diagram is offered in Figure 4-7. When utilized in conjunction with an off-chip 1 Meg-ohm resistor shunted by 0.1μF of capacitance, the circuit operates as an integrator. The source resistance seen by the configuration is the 5K-ohm load resistance in the output circuit of the detector-multiplier network. Since these source resistances are balanced, the electrical effects of nonzero input biasing currents are all but completely cancelled.

4.6.2 Comparator

Figure 4-8 displays the comparator circuit. The output collector is capable of drawing up to 10 milliamperes of current. With appropriate resistive load and supply voltage, the circuit can be rendered compatible with TTL or 10 volt CMOS/SOS.

4.7 Code Reclocking Register

The code tracking subcircuit in Figure 2-6 requires a code that is alternatively switched from 1/2 bit leading (early code) to 1/2 bit delayed (late code) with respect to the prompt code. The terminology herewith is such that the prompt code is taken to be the correct code.

4.7.1 Logic Diagram

The logic diagram of the code reclocking register shown in Figure 4-9 is appropriate for the generation of the early/late code. It also reclocks the code to ensure a differential signal possessed of equal bit lengths, equal rise and fall times, and proper voltage levels for mixer interface.

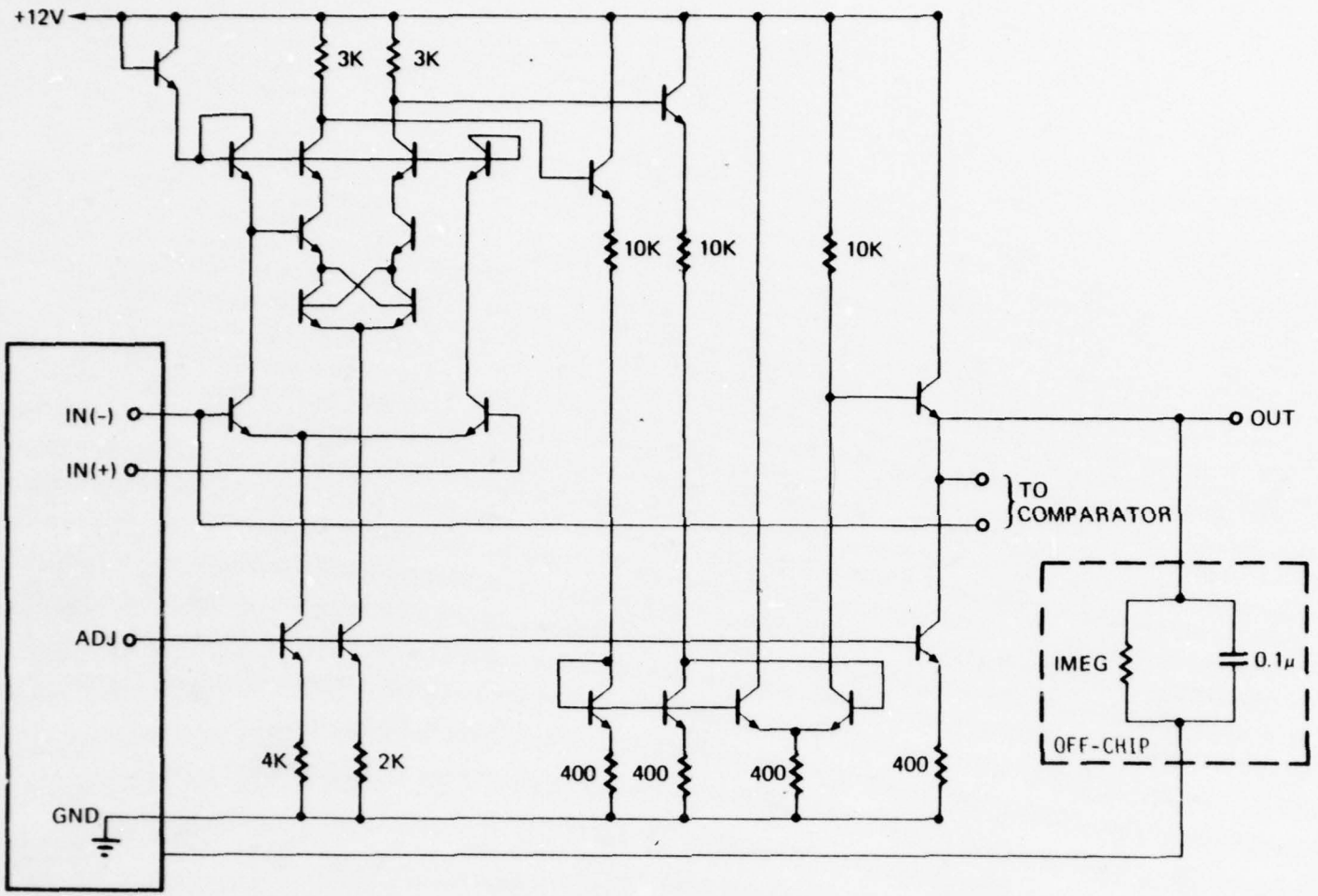


Figure 4-7 Operational Amplifier with Off-Chip Elements to Realize Integrating Function

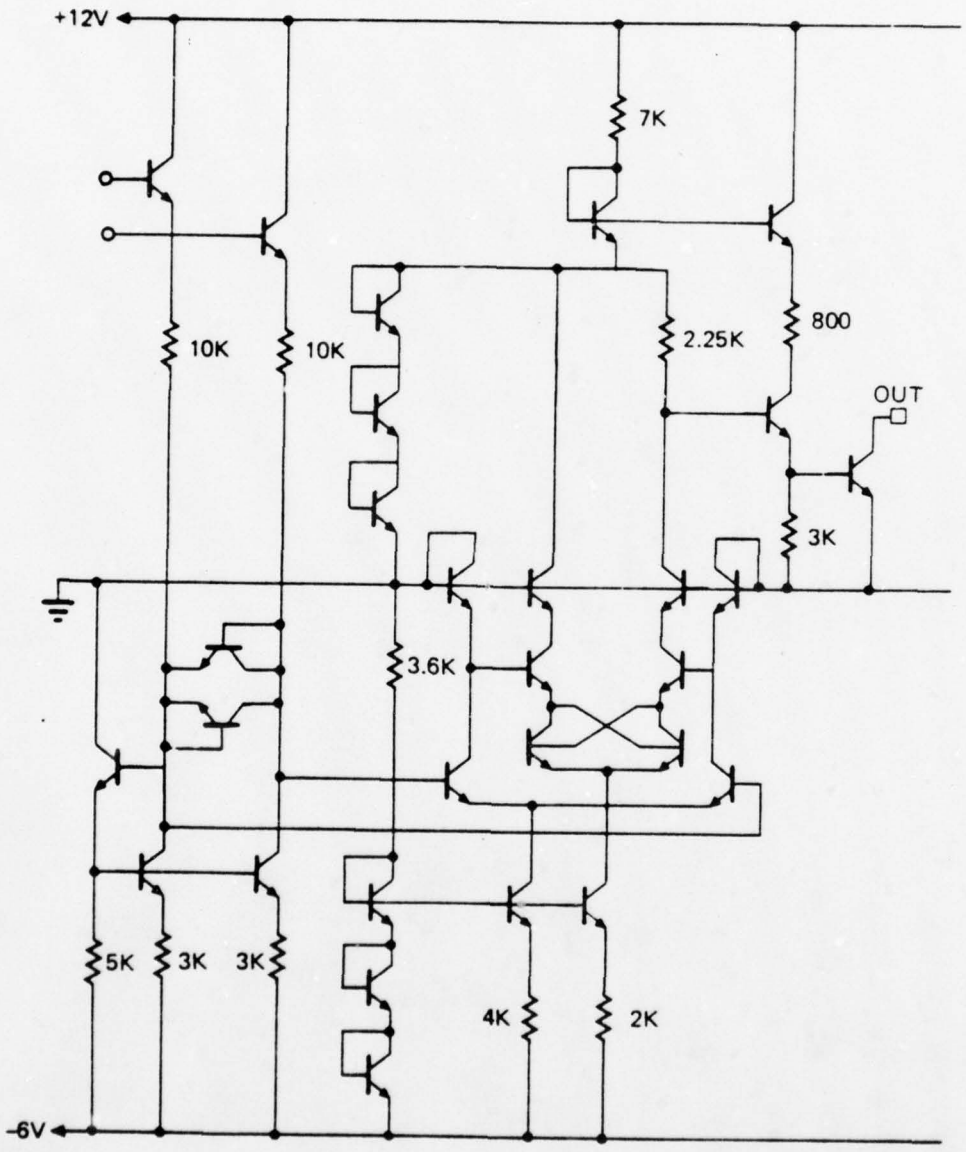


Figure 4-8 Comparator Circuit

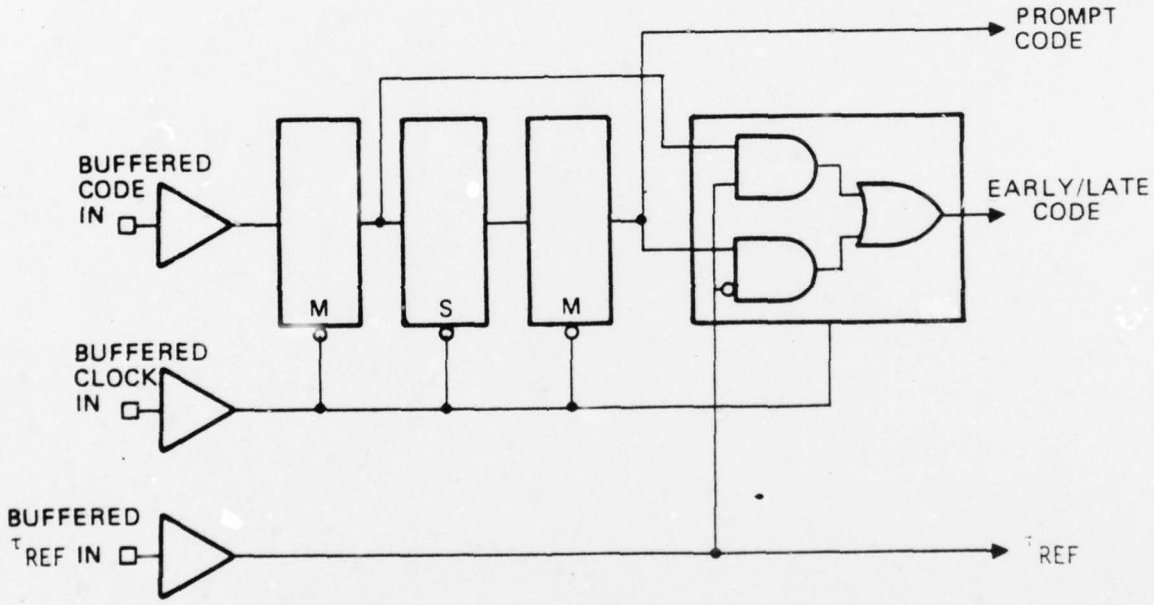


Figure 4-9 Logic Diagram of Code Reclocking Register

4.7.2 Low-Level Differential Switch

The operation of each switch in the logic diagram of Figure 4-9 can easily be understood by a cursory study of the low-level differential latch exemplified in Figure 4-10. When $\overline{\text{CLOCK}}$ signal is high, the output tracks the input; when CLOCK signal is low, the output remains constant. The voltage swing across the collector load resistors is typically 200mV, so that charge storage effects in the collector-base junctions is negligible. The latch shown is a master, the slave latch has reversed clock polarity. The input differential pair (T1, T2) may be replaced by any appropriate current-steering logic circuit such as the multiplexer in the fourth latch of the code reclocking register. In such a case, the inputs to the lower levels of the logic circuit must be appropriately level-shifted.

4.7.3 Code Reclocking Circuit

The pertinent schematic diagram is supplied in Figure 4-11. The first three latches, comprised of Q1 through Q18 and Q29 through Q31, mirror the low level logic circuit of Figure 4-10. The fourth latch (Q19 through Q28 and Q32) comprise a multiplexer.

4.8 Register Buffer

The register buffer of Figure 2-6 is depicted schematically in Figure 4-12. The code, clock, and τ_{REF} buffers provide the appropriate level shifts and output voltage excursions commensurate with reliable operation of the code reclocking register and associated code tracking loop.

4.9 Comments and Status

The GPS test chip discussed and defined schematically in the foregoing subsections is currently undergoing processing. Chips are tentatively scheduled for test availability in November. Test planning is well underway, and appropriate test fixturing is being designed and procured.

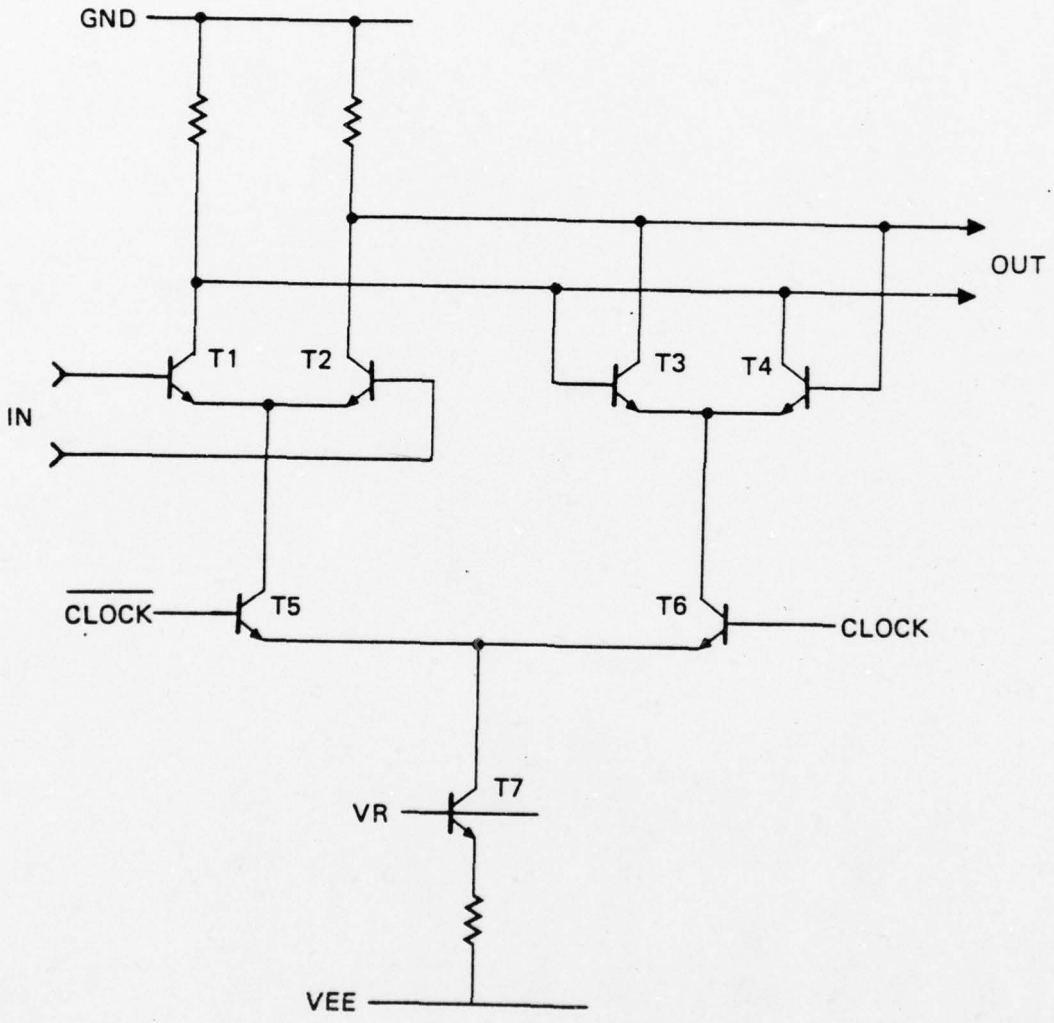


Figure 4-10 Low-Level Differential Latch

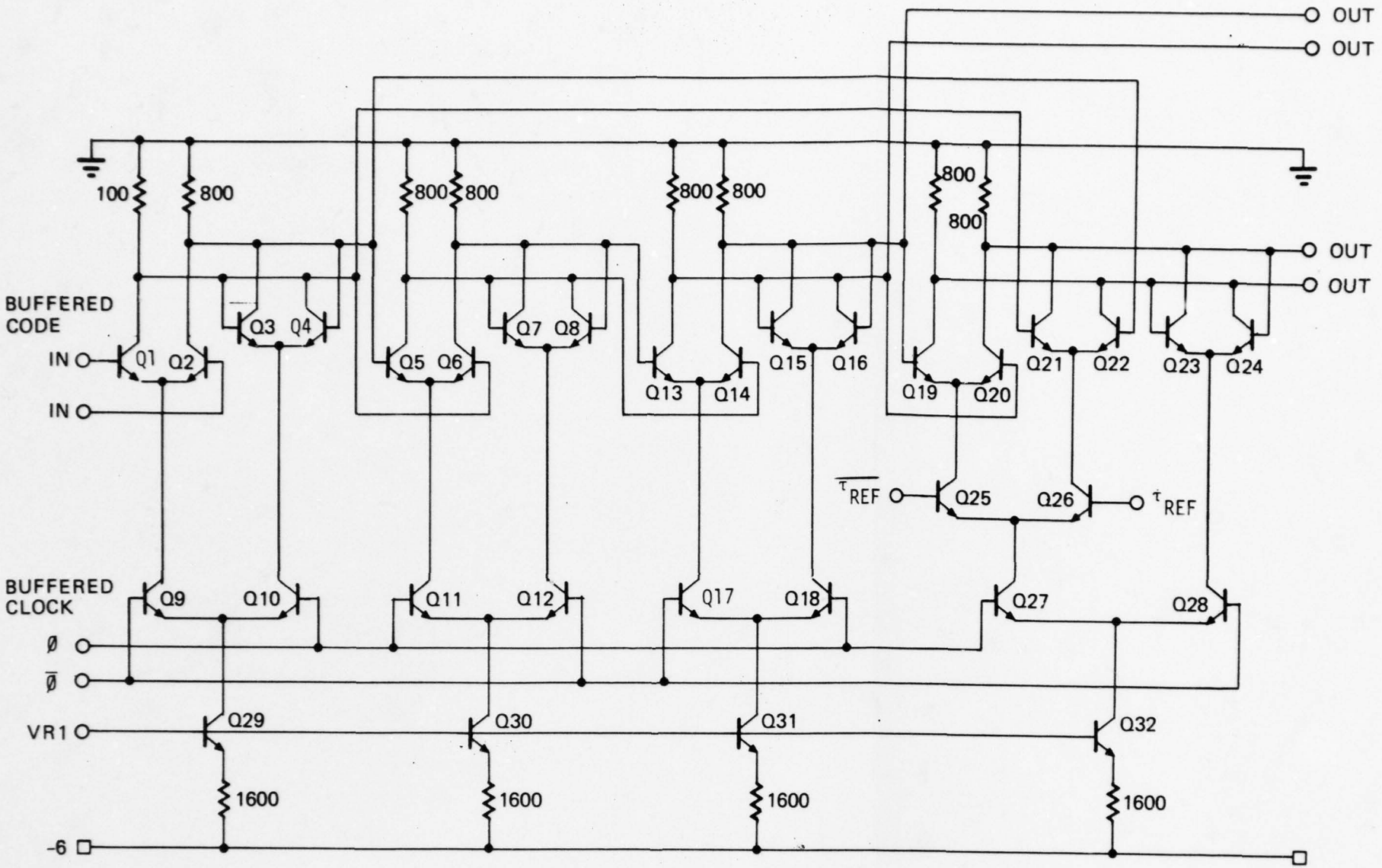


Figure 4-11 Schematic Diagram of Code Reclocking Register

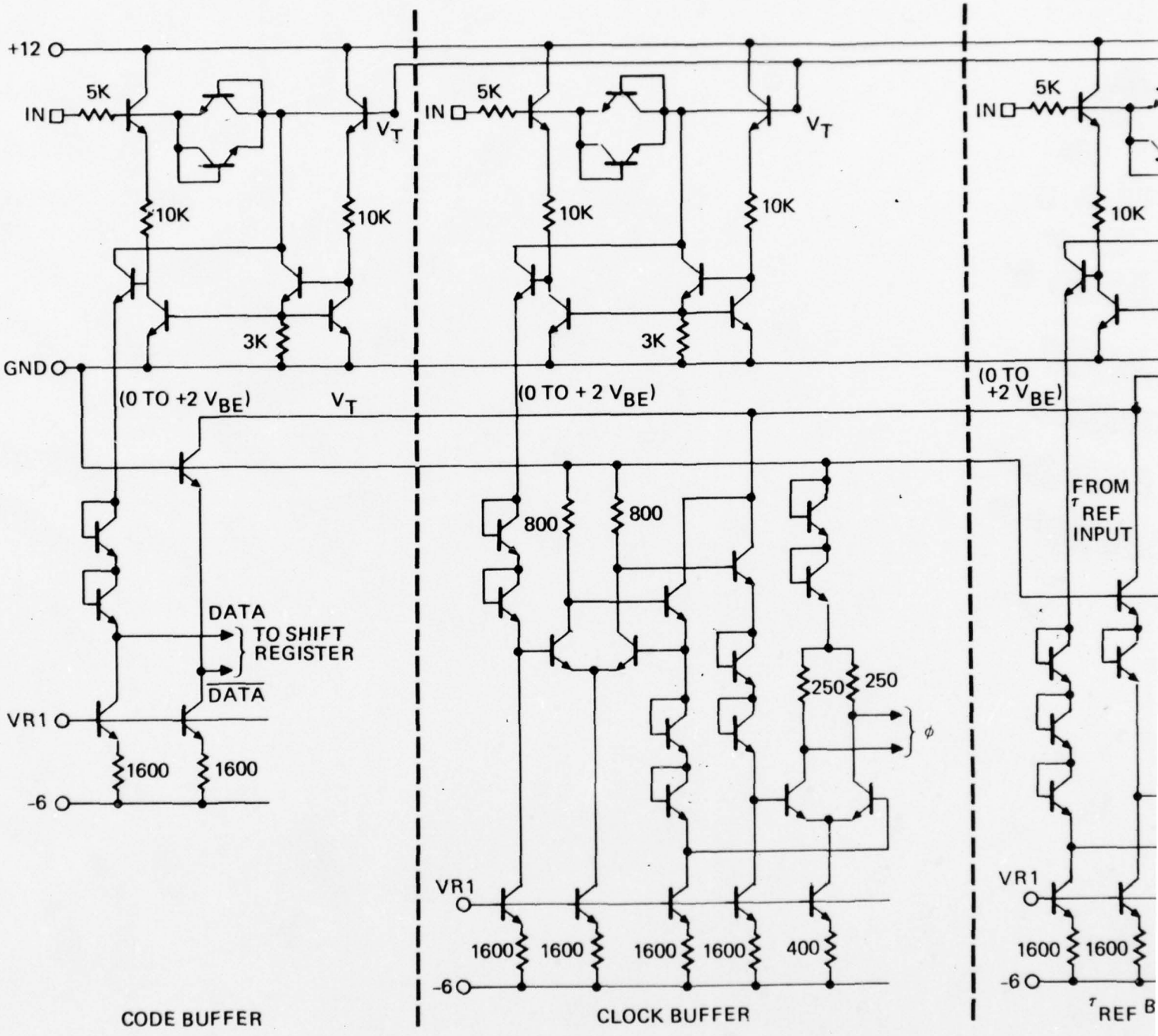

+12
IN
5K
10K
10K
3K
V_T
GND
(0 TO +2 V_{BE})
DATA
TO SHIFT REGISTER
$\overline{DATA}$
VR1
1600
1600
-6
CODE BUFFER
800
800
250
250
ϕ
400
CLOCK BUFFER
FROM τ REF INPUT
τ REF B

Figure 4-

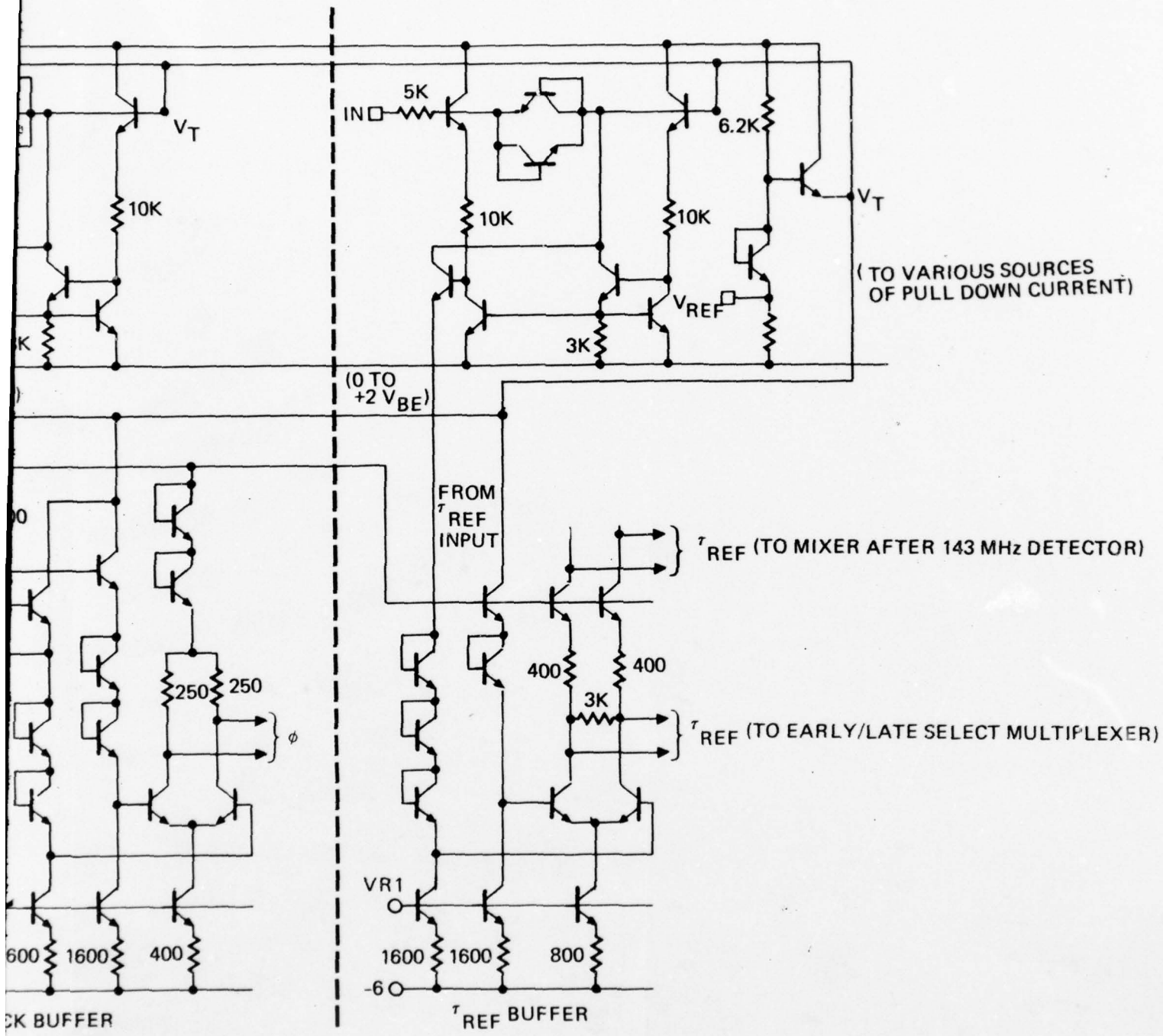


Figure 4-12 Schematic Diagram of Register Buffer Circuit

5.0 FUTURE NEAR TERM WORK

There are three areas of research and development emphasis in the immediate near term: (1) building block circuit development, (2) investigation of optimized wideband multiport interstage matching configurations, and (3) implementation of efficient computer-aided analysis and device modeling techniques.

5.1 Building Block Circuits

Six basic types of circuits are currently contemplated. These are a low noise preamplifier, automatic gain control amplifier, balanced four-quadrant analog multiplier, voltage controlled oscillator, Costas demodulator, and phase logic demodulator. The frequency range to which these circuits are to be receptive is 70 MHz-to-1600 MHz. However, the upshot of cognate TASK 1 studies strongly suggests that circuits intended for operation at frequencies below approximately 700 MHz are significantly easier to realize than are circuits destined for exposure to frequencies above 700 MHz. For frequencies in excess of approximately 700 MHz, interstage lossless matching networks are invariably mandated. Owing to inherent difficulties in the monolithic fabrication of matching networks having reliable and reproducible electrical characteristics and since there is a large demand for communication circuits operating at frequencies below 700 MHz, the current mode of thinking is to realize two forms of each of the aforementioned building block circuits. In particular, a "low" frequency version (<700 MHz) and a "high" frequency version of each block is to be developed. This thinking can change drastically if attempts at synthesizing active element lossless matching networks prove successful.

5.2 Active Matching

The interstage matching configurations currently employ floating (ungrounded) inductors and capacitors. Fortunately, the required capacitors are generally small and relatively easy to synthesize monolithically. But even small inductors consume exorbitantly large chip area and unless one terminal of each required inductor is at AC ground, they cannot

be realized actively at the frequencies appropriate to GPS. Accordingly, there is incentive to investigate the possibility of designing active versions of lossless matching networks exuding nonfloating inductors. The optimal matching network must be capable of achieving impedance matches over wide frequency ranges, as opposed to realization of matches at but a single frequency. This problem is genuinely difficult and indeed, there is some justification for believing that it is insoluble for certain special cases of circuit operation.

5.3 Computer-Aided Analysis

Computer-aided circuit analysis is the only practical tool for the design of circuits operating at GPS frequencies. Accordingly, continuing attention must be paid to any required device model alterations that ensure a close match between measured OAT characteristics and predicted circuit performance. This task is particularly critical in view of contemplated continuing improvements in OAT processing techniques.

In concert with established OAT transistor parameter determination techniques, a parameter catalog for all devices characterized thus far is being compiled. In addition to listing SPICE-2 model parameter values, the catalog is to contain all measured data and statements pertaining to the operational range of validity for all parameters quoted. The catalog is to be updated continually as more devices become available for characterization.

A program is being developed peripherally to SPICE to store all available model parameters. When operational, this external device library will enable SPICE users to input parameter sets into their simulations without having to input individual model parameters for each device used. The user will be able to input a device type into his simulation and in doing so, the parameter file for that device will automatically be inputed into the program for the circuit undergoing simulation.

Finally, on-chip parasitics are currently being analyzed. Present thinking infers that these parasitics can be characterized by a short circuit admittance matrix whose measureable elements reflect node-to-ground and node-to-node RC coupling. If this thinking bears fruit, the admittance matrix can be merged externally with the intrinsic SPICE nodal admittance matrix, thereby rendering plausible the incorporation of on-chip parasitic influences on nominal circuit behavior.

6.0 REFERENCES

1. "An Improved Global Positioning System (GPS) Receiver for Navy Use," TRW Report No. 32416.000, March 20, 1978.

2. J. J. Ebers and J. L. Moll, "Large-Signal Behavior of Junction Transistors," Proceedings of the IRE, Vol. 46, pp. 1141-1152, November 1952.

3. J. Choma, Jr., "A Spectral Density Approach to Noise Performance Calculations," Proceedings of the IEEE Region 6 Conference, April 1969.

4. J. F. Gibbons, Semiconductor Electronics. New York: McGraw-Hill Book Company, Inc., 1966, p. 816

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APPENDIX

TASK 1 REPORT

PREFACE - APPENDIX

This appendix documents the results of the TASK 1 component of contractual work performed under Navy Contract N00123-77-C-1045. The work is sponsored by the Naval Electronic Systems Command, Washington, D.C., by Mr. Nathan Butler and Mr. Larry Sumney of the Electronics Technology Division, ELEX 304. The contract monitor is Mr. C. A. West, Navan Ocean Systems Center, Code 923, San Diego, California. The work is being conducted by the Microelectronics Center of TRW Defense and Space Systems Group. The principal TRW investigator and author of this report is Dr. John Choma, Jr., who reports directly to Dr. Barry Dunbridge, Director of the Microelectronics Center.

A complete list of all technical personnel who have contributed to the conduct of TASK 1 is too lengthy for inclusion herewith. However, the author would be guilty of obvious oversight if he did not acknowledge the dedication and consistent creativity of a few of his colleagues. To this end, the author expresses his sincere appreciation of the exemplary endeavors of D. Claxton, A. Cosand, and G. McIver. He also thanks B. Dunbridge and L. Fletcher for establishing an administrative environment conducive to successful conduct of the state-of-the-art research and development demanded by this contract.

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CONTENTS

LIST OF ILLUSTRATIONS - APPENDIX

LIST OF ILLUSTRATIONS (CONTINUED)

1.0 INTRODUCTION

In September of 1977, TRW DSSG undertook a three year program to use the Oxide Aligned Transistor (OAT) fabrication technology in the development of circuit techniques and circuit building block configurations appropriate to the satisfaction of system requirements for analog circuits operating at signal frequencies through L-band. The program, sponsored by the Naval Ocean Systems Center, under contract N000123-77-C-1045, is configured in terms of six (6) distinct tasks.

In TASK 1, basic circuit technique development, the object is to develop analog circuit design methodologies which efficiently exploit OAT monolithic processes. In particular, circuits amenable to large scale integration (LSI) are to be developed in such a way as to insure maximal performance capability at minimal power consumption. In TASK 2, a GPS receiver system/module interface study is performed and a full GPS receiver is configured using the RF building blocks to be developed in TASK 3 of this program. Consistent with this configuration a GPS receiver test chip is to be designed, fabricated, tested, and delivered. General purpose, universal RF circuit building blocks are specified and designed in TASKS 4 and 5. A circuit family incorporating a wide range of specifications is to be designed to verify the worst-case set of design specifications. This analytical, empirical, and design information provides the means for applying circuit building blocks to a wide range of Navy requirements. Circuits from the test patterns are to be tested and evaluated. Ultimately, a completely tested receiver breadboard is to be delivered to the Navy.

This report documents the results of studies undertaken in TASK 1 of the contract. The intent of the report is to provide both circuit theoretic and pragmatic monolithic circuit design information on broadbanded linear amplifiers, sophisticated mathematical models of OAT transistors for realistic and reliable computer-aided analysis and design, electrical noise characteristics of OAT transistors, the degrading effects of various on-chip coupling parasitics, optimal analog multipliers, and optimal demondulator circuits.

It should be pointed out that all of the work discussed in this report is not exclusively supported under the present Navy contract. In particular, certain tasks implicit in the broadbanding work addressed in Section 2.0 is supported by TRW internal research and development (IRAD) funds. Virtually all of the raw data required to expedite the transistor modeling endeavors discussed in Section 3.0 derives from a previous Navy contract (N000123-76-C-1419), and a portion of the theoretical background leading to the final model is supported by IRAD dollars. IRAD money also supports the noise work in Section 4.0, all testing associated with both the coupling details in Section 5.0, the analog multiplier work appearing in Section 6.0, and most of the demodulator studies of Section 7.0.

2.0 BROADBANDING

A broadbanded active circuit is one which is capable of providing adequate voltage, current, or power gain over the widest possible range of signal frequencies. The primary deterrent to a wideband frequency response in a monolithic bipolar junction transistor (MBJT) amplifier is charge stored in the immediate neighborhood of either transistor junction. This stored charge is a direct ramification of the simple fact that charge injected into the base region of an MBJT cannot be transported instantaneously to the collector region. Rather, the motion of minority charge carriers is governed by the fundamental laws of diffusion and drift[1]. If, as in the case of low charge injection from emitter-to-base, charge transport is dominated by diffusion phenomena, the primary frequency response limitation is the so-called minority carrier transit time, τ_{F0}. This parameter is a measure of the average time required by a minority charge carrier to traverse the field neutral region of the base from the base edge of the emitter-base depletion region to the base edge of the collector-base depletion region. In narrow base devices, it varies nominally as the square of the width of the field neutral base region, and it is inversely proportional to the average diffusivity of the base.

If the collector-base junction is not strongly back biased and/or the base-emitter junction is substantially forward biased, the concept of a field neutral base is obscure, since the minority charge concentration in the base at any instant of time is comparable to, or in excess of, the background (or majority) carrier concentration in the base. Under this so-called "high injection" condition, the minority carrier diffusivity increases sharply, and the nominal minority carrier transit time is no longer limited by τ_{F0}. Instead, charge motion is strongly influenced by the charge carrier drift mobility associated with local electric fields established in the base by the presence of enhanced charge concentration levels.

To the extent that charge storage due to diffusion and drift effects can be represented by simple linear capacitances at each MBJT junction, the problem of realizing broadband performance reduces to the problem of offsetting most of the deleterious effects of transistor junction capacitances. Fundamentally, one can attempt to solve this problem by (1) minimization of input or output signal voltage swings, (2) partial or complete cancellation of the network poles precipitated by MBJTs, and (3) neutralization of active element susceptances by either active or passive circuit components. In practice, an acceptable wideband amplifier invariably exploits all three of the foregoing methodologies and accordingly, a rigorous definition of the specific method by which a given amplifier is made to achieve wideband performance is rendered difficult, if not impossible. Independent of the design technique utilized, however, it must be made clear that ultimately, the bandwidth and concomittant gain-bandwidth product of an amplifier is limited by the errors implicit in modeling the stored charge associated with distributed diffusion and drift phenomena by a finite number of capacitances.

2.1 Differential Amplifiers

Perhaps the most ubiquitous of amplifiers found in linear monolithic realizations is the differential amplifier, which is symbolically illustrated in Figure 2-1. If circuit linearity is presumed, superposition theory may be used to write

$$V_o(s) = A_1(s)V_1(s) + A_2(s)V_2(s), \tag{2-1}$$

where $V_1(s)$ and $V_2(s)$ are transforms of the applied signal voltages, $V_o(s)$ is the transform of resultant output voltage, and $A_1(s)$ and $A_2(s)$ are transfer functions determined by the elements embedded within the topology comprising the differential configuration. It is to be understood that $V_1(s)$ and $V_2(s)$ are monitored with respect to a common ground, while $V_o(s)$ may be differentially derived or established with respect to the common ground. If

$$V_d(s) = V_1(s) - V_2(s) \tag{2-2}$$

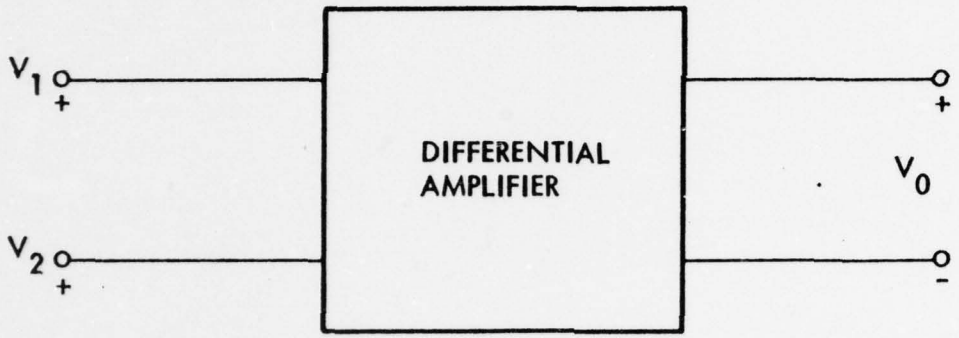

Figure 2-1 Symbolic Representation of Differential Amplifier

symbolizes the differential input signal voltage, and if

$$V_c(s) = \frac{1}{2}[V_1(s) + V_2(s)] \tag{2-3}$$

connotes the average or "common mode" input signal voltage, (2-1) is expressible as

$$V_o(s) = A_d(s)V_d(s) + A_c(s)V_c(s). \tag{2-4}$$

In (2-4),

$$A_d(s) = \frac{A_1(s) - A_2(s)}{2} \tag{2-5}$$

and

$$A_c(s) = A_1(s) + A_2(s) \tag{2-6}$$

respectively represent the differential and common mode gains. Equation (2-4) can also be cast in the form,

$$V_o(s) = A_d(s)\left\{1 + \frac{1}{\rho(s)} \frac{V_c(s)}{V_d(s)}\right\} V_d(s) \tag{2-7}$$

where $\rho(s)$, the common mode rejection ratio (CMRR) is given by

$$\rho(s) = \frac{A_d(s)}{A_c(s)}. \tag{2-8}$$

Two important points surface at this juncture. First, if $\rho(s)$ is infinitely large, the output of the differential amplifier is incapable of responding to a component signal that is common to both input signals, $V_1(s)$ and $V_2(s)$. An infinitely large CMRR characteristic is especially desirable if $V_1(s)$ and $V_2(s)$ derive from sources that supply a signal superimposed on quiescent voltages of identical strength. Observe that for a desired differential mode gain, $\rho(s)$ can be made infinitely large if $A_2(s)$ is the negative of $A_1(s)$. This is to say that infinite CMRR in Figure 2-1 requires that the gains, $V_o(j\omega)/V_1(j\omega)$ and $V_o(j\omega)/V_2(j\omega)$ be identical in magnitude, but phase shifted by 180° for all radial signal frequencies, ω.

The second noetworthy point is the fact that for equal output signal voltages, each input of the differential configuration need by driven with only one-half the signal voltage that is required of a single-ended amplifier having comparable voltage gain. In order to confirm this significant assertion, assume $\rho(s)$ is infinitely large, $V_1(s) = V_Q + V_S(s)$, and $V_2(s) = V_Q - V_S(s)$. Then (2-7) becomes

$$V_o(s) = 2A_1(s)V_s(s).$$

For an amplifier with single ended input, $A_2(s) = 0$, and (2-1) delivers

$$V_o(s)\Big|_{A_2 = 0} = A_1(s)[V_Q + V_S(s)].$$

Observe that the differential gain in the first case above is twice as large as the gain for the signal component of output voltage developed in the single-ended input amplifier. Additionally, note that the common mode signal, whose transform is symbolized in the above equations by V_Q, must be filtered from the net output voltage in a single-ended input amplifier, whereas the common mode signal is automatically suppressed by the infinitely large CMRR ostensibly achievable in differential amplifiers.

2.1.1 Simple Differential Pair

The simplest circuit capable of approximating a differential amplifier is the differential pair offered in Figure 2-2. For simplicity, the complete biasing network is not shown, both transistors are assumed identical, and both bases are excited by voltage sources having identical terminating resistances. Additionally, both input voltages $V_1(s)$ and $V_2(s)$, and the desired output voltage, $V_o(s)$, are monitored with respect to ground.

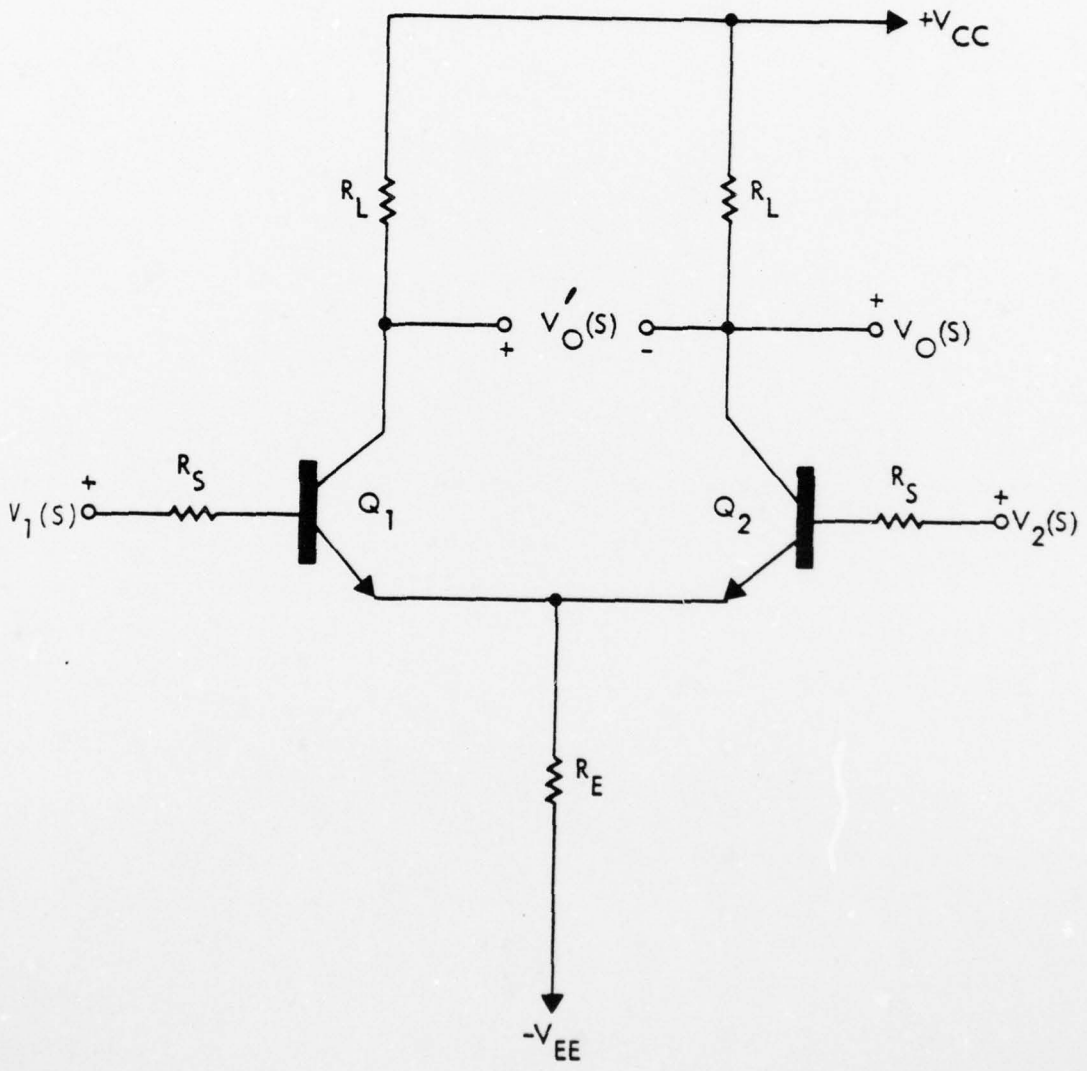

Figure 2-2 Simple Differential Pair

A small-signal, low frequency analysis of the circuit in Figure 2-2 shows that

$$A_d(s) = \frac{V_o(s)}{V_d(s)} = \frac{\beta_o R_L}{2(R_S + r_b + R_{pi})} , \tag{2-9}$$

$$A_c(s) = \frac{V_o(s)}{V_c(s)} = - \frac{\beta_o R_L}{R_S + r_b + R_{pi} + 2(\beta_o + 1)R_E} , \tag{2-10}$$

whence

$$\rho(s) = - \frac{R_S + r_b + R_{pi} + 2(\beta_o + 1)R_E}{2(R_S + r_b + R_{pi})} . \tag{2-11}$$

In (2-9) through (2-11), r_b is the small-signal resistance of the MBJT intrinsic base, β_o is the small-signal common-emitter short circuit current gain, and R_{pi} is the diffusion resistance of the base-emitter junction. As verified in Section 3.0, this latter small-signal element is given approximately by

$$R_{pi} \simeq \frac{\beta_o V_T}{I_{CQ}} , \tag{2-12}$$

where V_T is the thermal voltage of the junction (25.875 millivolts at room temperature) and I_{CQ} is the quiescent collector current flowing through each transistor. At I_{CQ} = 4 milliamperes, and taking r_b = 65 ohms, β_o = 45, R_S = 50 ohms, R_E = 750 ohms, and R_L = 100 ohms, typical values of the foregoing three quantities are

$$A_d(s) = 5.54 = 14.87\text{dB},$$

$$A_c(s) = -0.06 = -23.76\text{dB},$$

$$\rho(s) = -85.45 = -38.63\text{dB}.$$

2.1.2 Current Source Compensation

An inspection of (2-11) shows that $\rho(s)$ can be made substantially large if R_E is chosen to be a large resistance. Since R_E in Figure 2-2 must conduct the sum of quiescent transistor emitter currents, there are obvious practical limitations to this resistance value. The problem at hand is ostensibly solved if R_E is supplanted by a constant current source designed to conduct the required quiescent current level. The alternative differential amplifier realization is depicted in Figure 2-3, where the base of current source transistor Q_I is presumed to be excited by a thermally compensated quiescent voltage, V_{II}. The Thevenin resistance of this voltage source is R_I.

Unfortunately, state-of-the-art high frequency integrated circuit processes do not generally produce MBJTs that are capable of closely emulating idealized current source characteristics in the sense of infinitely large dynamic collector-to-ground impedance. In particular, the narrow base width and realitvely light epitaxial layer doping of these bipolar devices respectively contribute to significant conductivity modulation and base pushout. The cumulative effects of these and other related phenomena result in a strongly capacitive dynamic collector-to-ground impedance whose magnitude attenuates dramatically with increasing signal frequencies. Indeed, the effective collector-to-ground impedance of a current source may degrade so sharply with frequency that a simple, passive resistance, chosen to satisfy quiescent operating constraints, becomes a prudent approximation to a constant current source in high-frequency analog circuits.

The small-signal, single lump, hybrid-pi model of the current source in Figure 2-3 is depicted in Figure 2-4.* An ideal one ampere current generator is applied across collector-to-ground ports so that the resultant voltage, $V_c(s)$, developed across the collector is symbolically equal to the dynamic collector-to-ground impedance, $Z_o(s)$.

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* A detailed discussion of the model, and its large signal counterpart appears in Section 3.0 of this report.

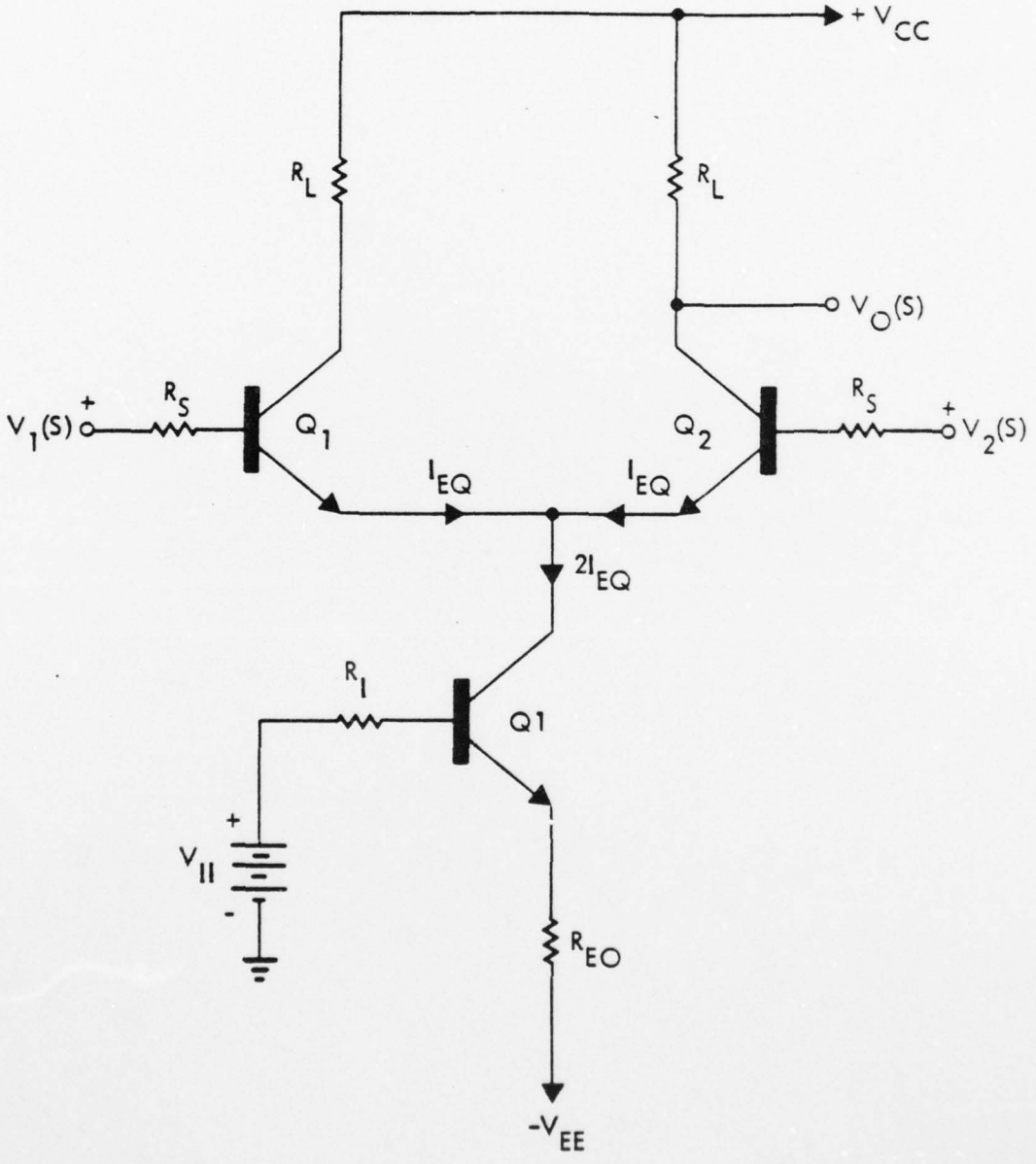

Figure 2-3 Current Source Compensation of CMRR Characteristics In Differential Amplifier

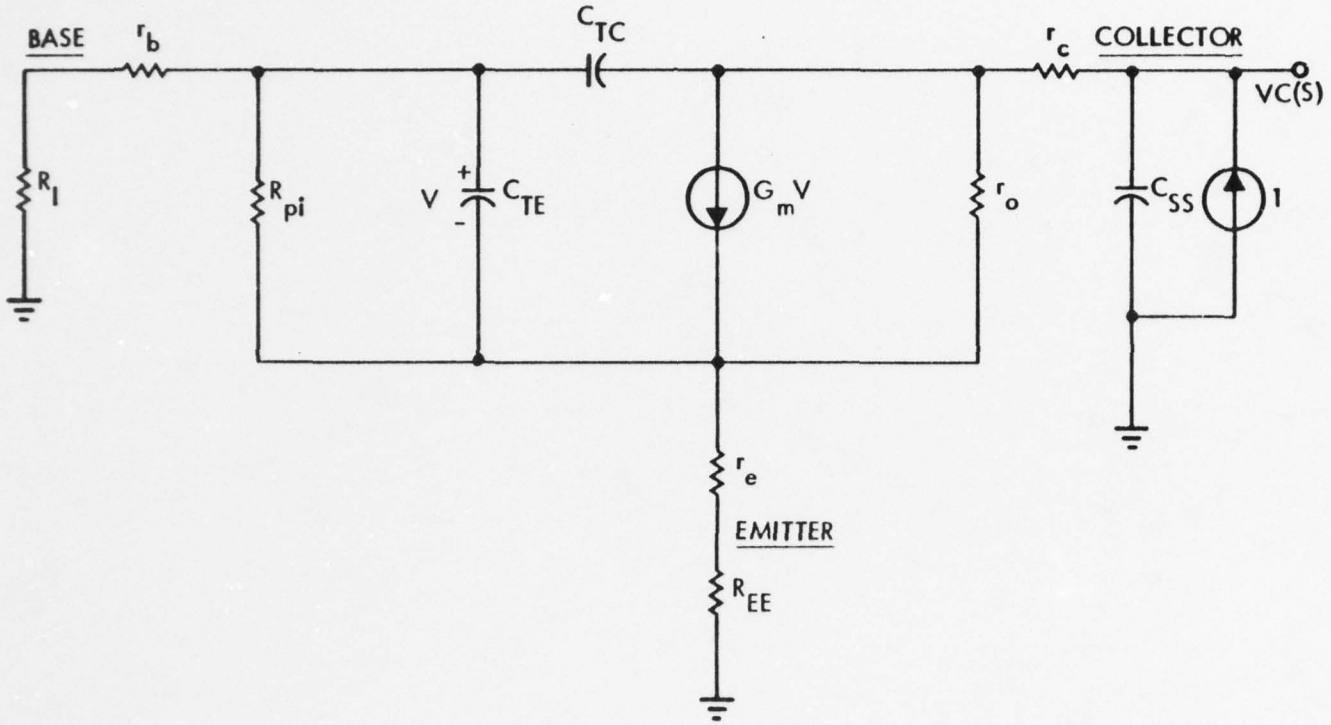

Figure 2-4 Small-Signal Hybrid-Pi Model of NPN Current Source. Capacitance C_{SS} pertains to the substrate, C_{TC} is the net collector junction capacitance, and C_{TE} is the total capacitance of the emitter junction.

It should be pointed out that the model of Figure 2-4 is applicable in both the low injection regime, where gain-bandwidth product f_T is a monotonically increasing function of collector current, and the high injection regimes, where gain and bandwidth degrade as a result of charge storage in the base and epitaxial layers.

The model shown in Figure 2-4 is redrawn for convenience as Figure 2-5, wherein, voltage source resistance R_I is combined with base resistance r_b to produce an effective base-to-ground resistance, R_{BB}. Similarly, R_{EE} is the net emitter-to-ground resistance.

The impedance, $Z_o'(s)$, seen to the left of output resistance r_o can be found by solving for the ratio, V_o'/I_o'. The equations of interest are

$$V_o' = \frac{1}{sC_{TC}}(I_o' - g_m V) + R_{BB}\left\{I_o - g_m V - \left(\frac{1}{R_{pi}} + sC_{TE}\right)V\right\} \qquad (2\text{-}12)$$

and

$$V = R_{BB}\left\{I_o' - g_m V - \left(\frac{1}{R_{pi}} + sC_{TE}\right)V\right\} - R_{EE}\left\{g_m + \frac{1}{R_{pi}} + sC_{TE}\right\}V. \qquad (2\text{-}13)$$

These equations can be cast into the form of a series interconnection of a frequency dependent resistor, $R_{BO}(s)$, and a frequency dependent capacitor, $C_{TO}(s)$; i.e.,

$$Z_o(s) = R_{BO}(s) + \frac{1}{sC_{TO}(s)}\ , \qquad (2\text{-}14)$$

where

$$R_{BO}(s) = \left\{\frac{1 + (g_m + 1/R_{pi})R_{EE} + sR_{EE}C_{TE}}{1 + (g_m + 1/R_{pi})(R_{BB} + R_{EE}) + s(R_{BB} + R_{EE})C_{TE}}\right\}R_{BB} \qquad (2\text{-}15)$$

and

$$C_{TO}(s) = \left\{1 + \frac{K_{TO}}{1 + s/\omega_{TO}}\right\}C_{TC}. \qquad (2\text{-}16)$$

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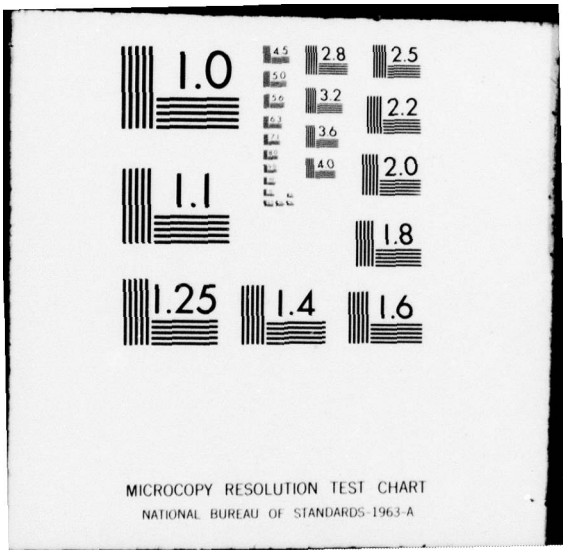
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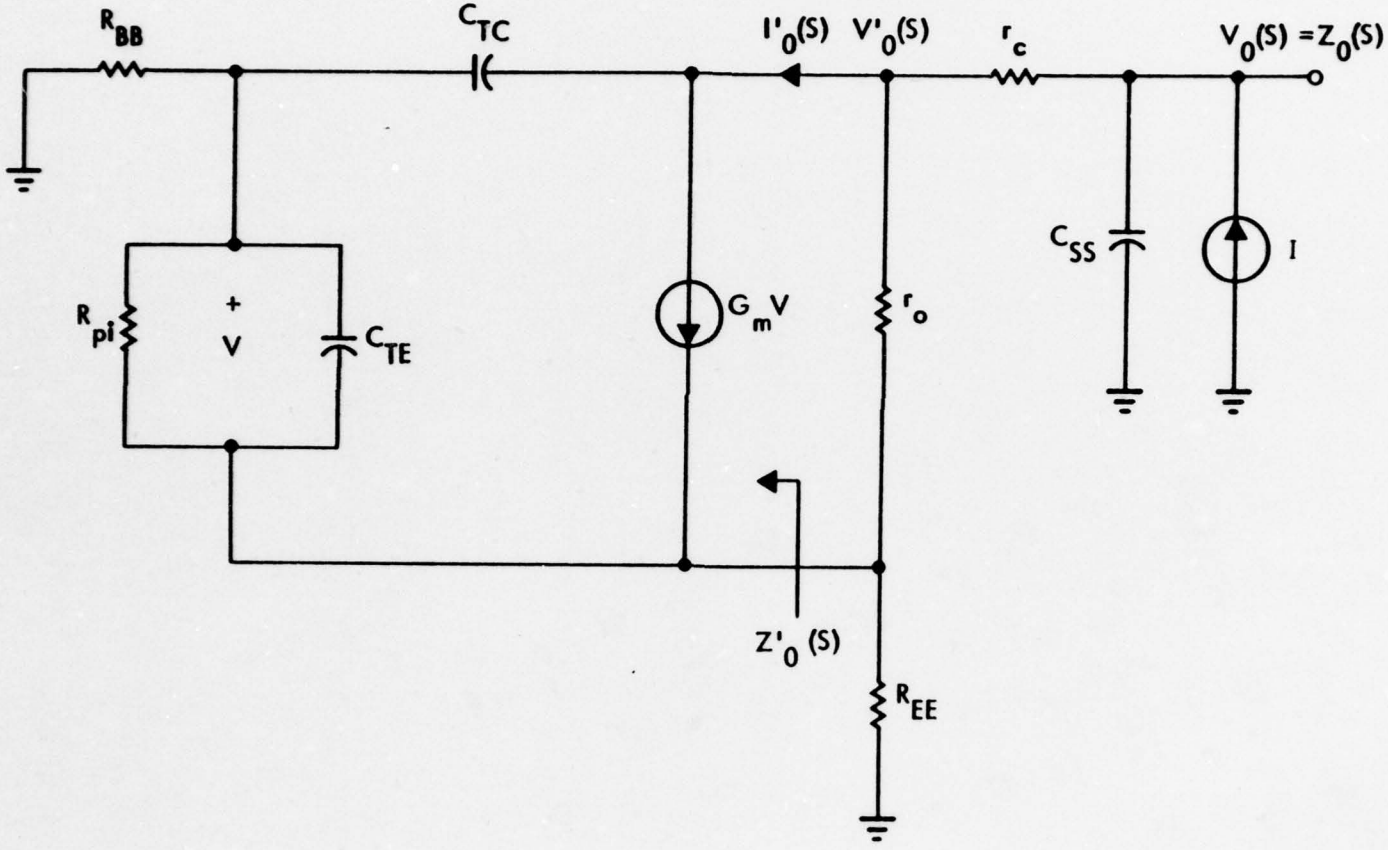


Figure 2-5 Small-Signal Current Source Model

In (2-16),

$$K_{TO} \triangleq \frac{g_m R_{BB}}{1 + g_m R_{EE} + \frac{R_{BB} + R_{EE}}{R_{pi}}} \tag{2-17}$$

$$\omega_{TO} \triangleq \frac{1 + g_m R_{EE} + (R_{BB} + R_{EE})/R_{pi}}{(R_{BB} + R_{EE})C_{TE}} . \tag{2-18}$$

It is to be observed that for forward transconductances which conform to the inequality,

$$g_m >> \frac{1}{R_{EE}} (1 + \frac{R_{BB}}{R_{pi}}) + 1/R_{pi}, \tag{2-19}$$

$$K_{TO} \simeq \frac{R_{BB}}{R_{EE}} , \tag{2-20}$$

$$\omega_{TO} \simeq \frac{g_m R_{EE}}{(R_{BB} + R_E)C_{TE}} = \frac{\omega_T}{1 + K_{TO}} . \tag{2-21}$$

The last result exploits the fact that the common emitter gain-bandwidth product of an MBJT is approximately equal to the ratio, g_m/C_{TE}. Thus, (2-16) implies that the effective capacitance seen at the intrinsic collector-to-ground port of a current source is a multiplied version of the collector junction capacitance. At low frequencies, the amount of this multiplication is approximately $(1 + R_{BB}/R_{EE})$ while for very high frequencies, the multiplication factor approaches unity.

It is also to be noted that the resistive portion, $R_{BO}(s)$, of impedance $Z_o^-(s)$ is virtually independent of frequency. For large g_m, (2-15) shows that

$$\lim_{s \to 0} R_{BO}(s) = R_{BB} || R_{EE}, \tag{2-22}$$

and for very high frequencies, precisely the same value is approached by $R_{BO}(s)$. This fact, coupled with the foregoing capacitance observations permits drawing the simplified small-signal current source model advanced in Figure 2-6. In a sense, the model is germane to worst case output impedance computations, since the capacitance shunting C_{TC} vanishes for sufficiently large frequencies. Resistance, r_o, in Figure 2-5 is tacitly connected between intrinsic collector and ground. It can be shown that this interconnection is valid, provided $R_{EE} << r_o$.

To the extent that r_o is a large resistance, output impedance $Z_o(s)$ in Figure 2-6 can be closely approximated by

$$Z_o(s) = r_o || \tilde{Z_o}(s), \tag{2-23}$$

where

$$\tilde{Z_o}(s) = \frac{1}{s(C + C_{SS})} + \left(\frac{C}{C + C_{SS}}\right)^2 \left[\frac{R}{1 + sRC_{SS}\left(\frac{C}{C + C_{SS}}\right)}\right]. \tag{2-24}$$

Equations (2-23) and (2-24) are representative of the driving point impedance for the equivalent circuit provided in Figure 2-7, with the understanding that

$$C_{eq} = C + C_{SS} = (1 + K_{TO})C_{TC} + C_{SS}, \tag{2-25}$$

$$R_K = \left(\frac{C}{C + C_{SS}}\right)^2 R = \left(\frac{C}{C + C_{SS}}\right)^2 \left[r_c + R_{BB} || R_{EE}\right], \tag{2-26}$$

$$C_K = \left(\frac{C + C_{SS}}{C}\right) C_{SS}. \tag{2-27}$$

The significance of the foregoing results is easily illustrated by numerical example. To this end, assume that R_{BB}, which is the sum of voltage source resistance R_I and intrinsic base resistance r_b is 450 ohms, $R_{EE} = R_{EO} + r_e = 110$ ohms, $r_c = 10$ ohms, and $C_{SS} = 0.35$ pF. If I_{EQ} in Figure 2-3) is 4mA, the current source conducts a collector current of 8mA, so that for transistor Q_I,

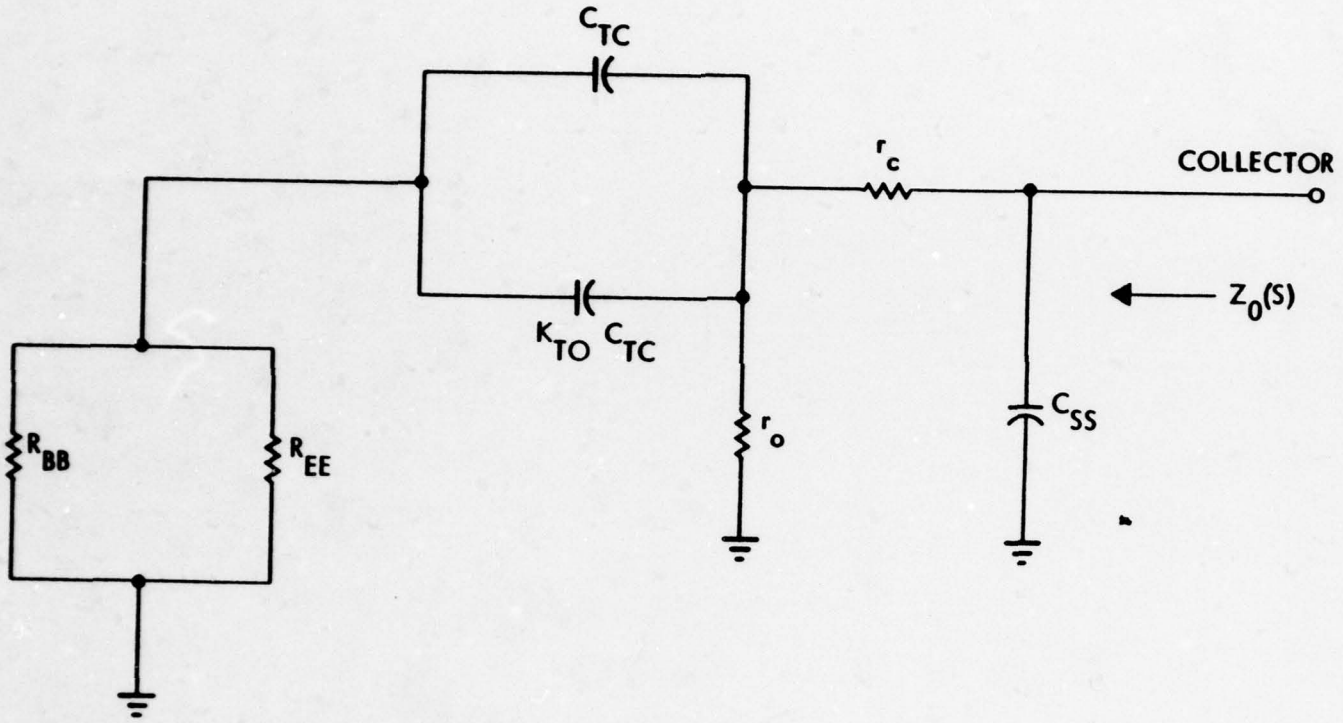


Figure 2-6 Simplified Circuit Model for an NPN Current Source Model is valid for frequencies less than $\omega_T/1 + K_{TO})$, where $K_{TO} = R_{BB}/R_{EE}$. Additionally, large forward gain is assumed.

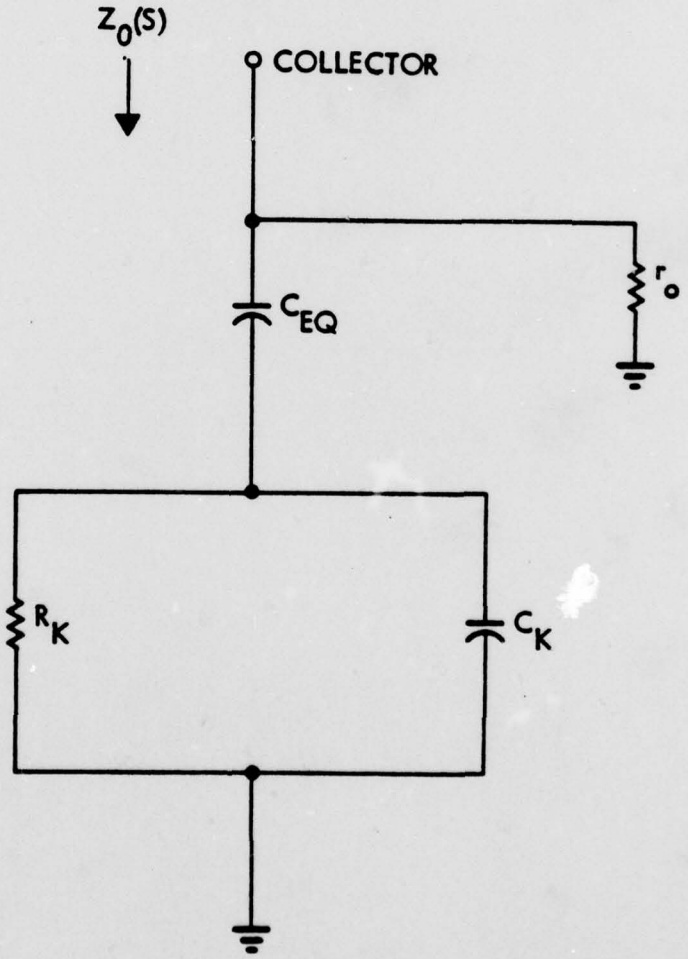


Figure 2-7 Approximate Small-Signal Equivalent Circuit of NPN Current Source for Frequencies Below ω_{TO}, as Defined By (2-21)

$$R_{pi} = \frac{\beta_o V_T}{I_{CQ}} = \frac{(45)(25.875)}{8} = 145.55 \text{ ohms},$$

while

$$g_m = \frac{\beta_o}{R_{pi}} = \frac{45}{145.55} = 309 \text{ mmhos}.$$

Finally, C_{TE} and C_{TC} may be taken respectively as 20 picofarads and 0.3 picofarads, thereby giving an effective gain-bandwidth product at the operating point of

$$f_T \simeq \frac{g_m}{2\pi(C_{TE} + C_{TC})} = 2.42 \text{ GHz}.$$

From (2-20),

$$K_{TO} = \frac{450}{110} = 4.09,$$

and by (2-21), the following calculations are appropriate for signal frequencies that are smaller than

$$f_{TO} = \frac{2.42}{1 + 4.09} = 475 \text{ MHz}.$$

Now, using (2-25) through (2-27),

$$C_{eq} = 1.88 \text{ pF}$$

$$R_K = 65.17 \text{ ohms},$$

$$C_K = 0.43 \text{ pF}.$$

Then at 400 MHz,

$$\tilde{Z_o}(j\omega) = \frac{1}{j\omega C_{eq}} + \frac{R_K}{1 + j\omega R_K C_K}$$

$$= 64.85 - j216.21 \text{ ohms} = 225.73\varepsilon^{-j73.30^\circ} \text{ ohms}.$$

If r_o = 3000 ohms, (2-23) provides

$$Z_o(j\omega) = 220.40\varepsilon^{-j69.27°} .$$

The foregoing discussion and numerical example vividly illustrates the impropriety of a current source at high signal frequencies. The fundamental problem is that the collector junction capacitance is, in effect, multiplied by a factor, $(1 + K_{TO})$, where K_{TO} is the ratio of the net resistance returning the base of the current source transistor to AC ground, to the net emitter-to-AC ground resistance. The undeniable conclusion is that the simple differential circuit shown in Figure 2-2 is significantly more adept at delivering acceptably large CMRR than is the rather commonly encountered configuration depicted in Figure 2-3.

2.1.3 Ideal CMRR Compensation

Although the analysis documented in the preceding section is fundamentally correct in the sense that it correctly conveys the impropriety of utilizing current sources in high frequency amplifier applications, the investigation performed is somewhat superficial in that high frequency dynamics in the differential pair are not included in the CMRR expression, equation (2-11). Accordingly, it is worthwhile to derive the nature of required CMRR compensation when high frequency dynamics in the differential pair are not negligible. To this end, the small signal equivalent circuit of Figure 2-2 is submitted in Figure 2-8. Homologous transistor operation is presumed, and each transistor is represented by its short circuit admittance parameter model. Each Y_{ij} in this model is a measurable parameter for all frequencies of interest and moreover, each Y_{ij} is expressible as an explicit function of the high frequency hybrid pi model discussed in Section 3.0. In the interest of generality, resistor R_E is replaced by admittance Y_E in the model of Figure 2-8. The problem herewith is to determine Y_E commensurate with zero output voltage response to common mode excitation at both amplifier input ports.

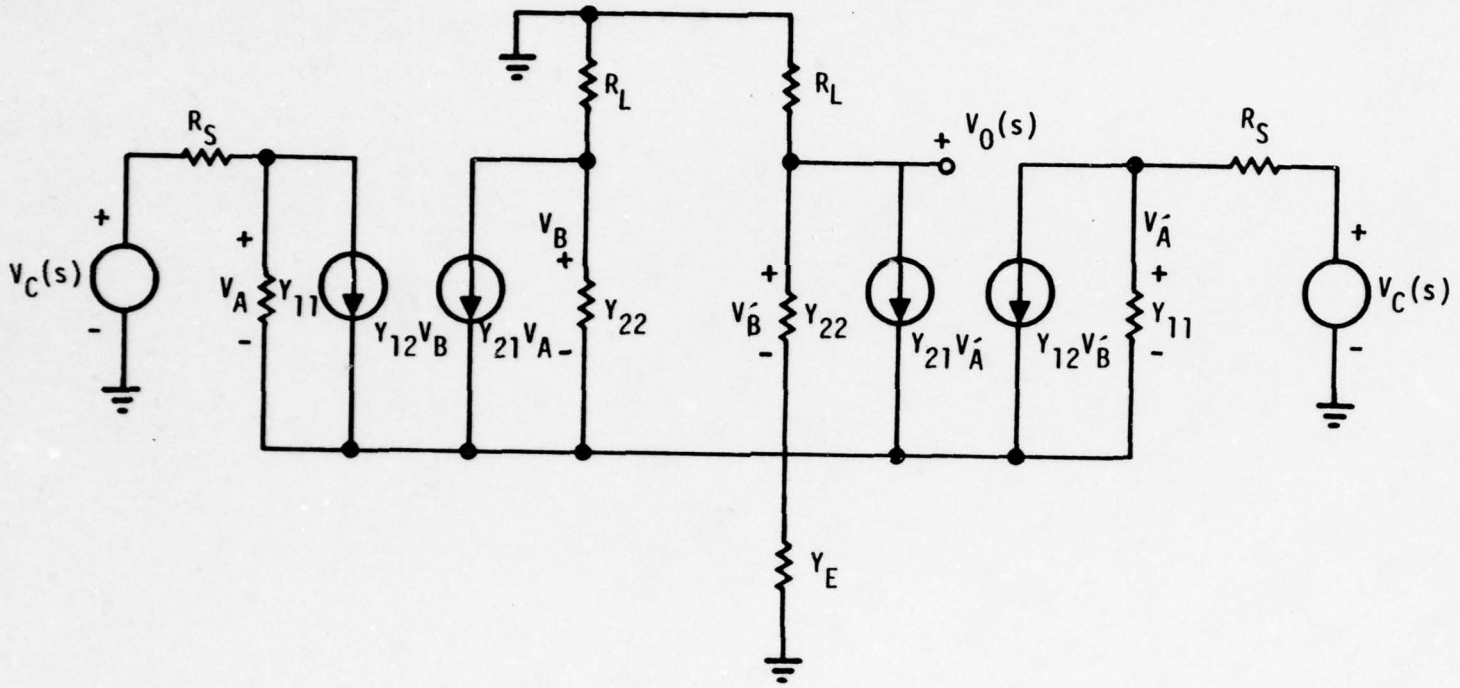


Figure 2-8 Y-Parameter Equivalent Circuit of Differential Amplifier shown in Figure 2-2. Note that both inputs are driven with the same voltage, $V_C(s)$.

Assuming homologous circuit elements, voltages V_A and V_B are, for common mode excitation, respectively identical to V_A' and V_B'. Note then that the currents through each load resistor are zero if

$$Y_{21}V_A = -Y_{22}V_B. \tag{2-28}$$

Since V_o is the voltage drop across R_L, (2-28) can be interpreted as both necessary and sufficient for infinitely large common mode rejection ratio.

Because of (2-28), the net current flowing through Y_E is $2(Y_{11}V_A + Y_{12}V_B)$. Thus for $\rho(s) = \infty$,

$$V_o(s) = 0 = V_2 + \frac{2(Y_{11}V_A + Y_{12}V_B)}{Y_E} \tag{2-29}$$

or equivalently,

$$2Y_{11}V_A = -(Y_E + 2y_{12})V_B. \tag{2-30}$$

Division of (2-29) by (2-30) eliminates V_A and V_B and leads to the design-oriented result,

$$Y_E = \frac{2}{y_{21}}\left[\text{DET}(Y_{ij})\right] , \tag{2-31}$$

where $\text{DET}(Y_{ij})$ connotes the determinant of the y-matrix

$$\bar{Y} = \begin{bmatrix} Y_{11} & Y_{12} \\ Y_{21} & Y_{22} \end{bmatrix} . \tag{2-32}$$

Equation (2-31) comprises a generalized solution for the emitter-to-AC ground admittance function conducive to $\rho(s) = \infty$. Observe that an ideal current source in the sense of $Y_E = 0$ (infinitely large dynamic impedance) is mandated only if $Y_{12} = Y_{22} = 0$. Since Y_{12} is a measure of intrinsic device feedback, the condition of $Y_{12} = 0$ implies zero collector-base junction capacitance. The condition, $Y_{22} = 0$, is tantamount to requiring infinitely large dynamic output impedance of each device utilized in the differential pair. Both of these conditions are pragmatically unrealistic, although, as shown in the next subsection of

material, the first constraint ($Y_{12} = 0$) can be closely approximated. If Y_{12} is indeed zero, (2-31) and (2-32) combine to deliver

$$Y_E = \frac{2}{Y_{21}}(Y_{11}Y_{22})$$

and since Y_{21}/Y_{11} is identical to the small signal, short circuit, common emitter current gain, $\beta(s)$,

$$Y_E = \frac{2Y_{22}}{\beta(s)} \tag{2-33}$$

is the emitter-ground dynamic admittance commensurate with $\rho(s) = \infty$.

Attempts at an active circuit realization of the admittance given by (2-33) have thus far proven unsuccessful. Observe that (2-33) constitutes a stringent requirement, for it infers that typical values of emitter-ground common mode impedance commensurate with $\rho(s) = \infty$ are quite large (of the order of 50 to 75 kiloohms at low frequencies).

2.1.4 Neutralization of Y_{12}

Consider the symbolic AC schematic diagram of Figure 2-9, which shows a transistor connected in shunt-shunt with a network having a single admittance incident with both the base and a phase inverting, unity turns ratio transformer coupled to the collector. Let the small-signal dynamic properties of the transistor be defined by the admittance representation,

$$\begin{bmatrix} I_1 \\ I_2 \end{bmatrix} = \begin{bmatrix} Y_{11} & Y_{12} \\ Y_{21} & Y_{22} \end{bmatrix} \begin{bmatrix} V_A \\ V_B \end{bmatrix}. \tag{2-34}$$

Inspection of the feedback network leads to

$$\begin{bmatrix} I_{F1} \\ I_{F2} \end{bmatrix} = \begin{bmatrix} Y_f & Y_f \\ Y_f & Y_f \end{bmatrix} \begin{bmatrix} V_A \\ V_B \end{bmatrix}. \tag{2-35}$$

Since $I_A = I_1 + I_{F1}$ and $I_B = I_2 + I_{F2}$,

$$\begin{bmatrix} I_A \\ I_B \end{bmatrix} = \begin{bmatrix} Y_{11} + Y_f & Y_{12} + Y_f \\ Y_{21} + Y_f & Y_{22} + Y_f \end{bmatrix} \begin{bmatrix} V_A \\ V_B \end{bmatrix} \tag{2-36}$$

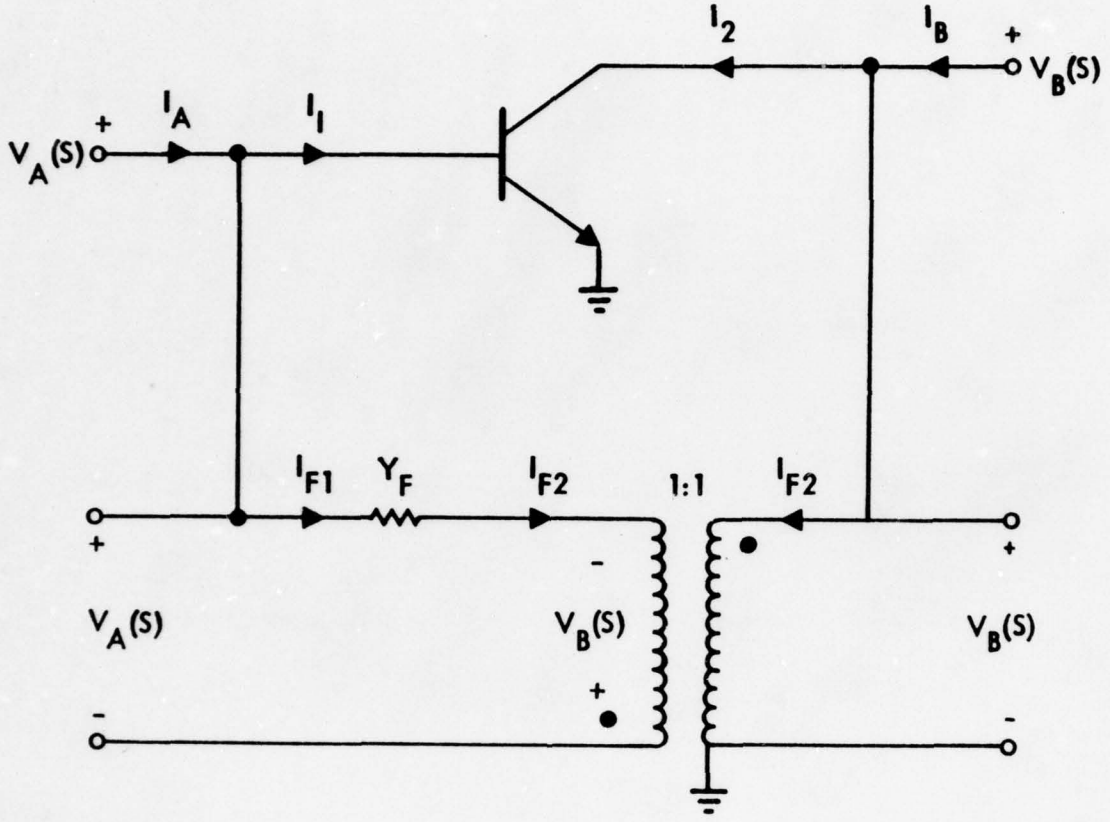


Figure 2-9 Symbolic Representation of Transistor Feedback Neutrallization Scheme

is the characteristic two port equation for the overall interconnection. Observe that if Y_f is chosen in accordance with

$$Y_f = -Y_{12}, \tag{2-37}$$

the overall network in Figure 2-9 is equivalent to an "effective" transistor possessed of no intrinsic feedback; that is,

$$\begin{bmatrix} I_A \\ I_B \end{bmatrix} = \begin{bmatrix} (Y_{11} - Y_{12}) & 0 \\ (Y_{21} - Y_{12}) & (Y_{22} - Y_{12}) \end{bmatrix} \begin{bmatrix} V_A \\ V_B \end{bmatrix}. \tag{2-38}$$

To the extent that Y_{11}, Y_{21}, and Y_{22} each have magnitudes that are substantially larger than $|Y_{12}|$, a comparison of (2-38) with (2-34) infers that the immediate effect of the shunt-shunt compensation proposed in Figure 2-9 is to neutralize intrinsic transistor feedback.

It can be shown that the feedback parameter, Y_{12}, for a transistor connected in common emitter orientation is

$$Y_{12} = -\frac{sK_1C_{TC}}{1 + s/\omega_b}, \tag{2-39}$$

with

$$K_1 = \frac{R_{pi}}{R_{pi} + r_b} \tag{2-40}$$

$$\omega_b = \frac{1}{(r_b||R_{pi})(C_{TE} + C_{TC})}. \tag{2-41}$$

From (2-37) and (2-39), the compensation required for feedback neutralization is

$$Y_f = \frac{sK_1C_{TC}}{1 + s/\omega_b}, \tag{2-42}$$

which is a positive real admittance function.

Although Y_f in (2-42) can be synthesized with passive components, it can also be synthesized actively for utilization in conjunction with the differential amplifier of Figure 2-2. In particular, note that Y_{12} is indigenous to the collector-base junction of a transistor and that signals applied to the bases are in phase with those developed at respective opposite transistors. These observations converge to the schematic diagram in Figure 2-10. Transistor QC1 serves to compensate Q1, since the base of QC1 is common to that of Q1 and the collector of QC1 is connected to the collector of Q2 which, for signal conditions, is 180° phase displaced from the signal established at the collector of Q1. In effect, Q2 serves as the required phase inverting transformer for the compensation admittance realized by the base-collector admittance of transistor QC1. Likewise, QC2 compensates the feedback inherent in transistor Q2. Observe that the collector-base bias voltages of all four collector-base junctions are identical if Q1 and Q2 operate under balanced quiescent conditions. If, in addition, R_E' is set to achieve identical collector currents in all four transistors, all four transistors exude identical small-signal parameter characteristics, thereby producing presumably excellent matching and tracking of the proposed compensation scheme.

Aside from simplifying the problem of achieving high CMRR without the use of active current sources, active feedback neutralization also serves to decrease the effective input capacitance seen at either input. In general, this capacitance is approximately the sum of the base-emitter junction capacitance and the Miller capacitance, $(1 + g_m R_L)C_{TC}$ [2]. By neutralizing C_{TC}, this capacitance is substantially reduced, particularly if large load resistance (R_L) is required to achieve high voltage gain.

2.1.5 Differential Quartet

While the circuit of Figure 2-10 is conducive to a broadband response, it does not adequately solve the problem of realizing very large CMRR since, as inferred previously, even ideal feedback neutralization mandates the implementation of a large dynamic impedance from emitter to AC ground.

Figure 2-10 Active Neutrallization of Transistor Feedback

The differential quartet shown in Figure 2-11 overcomes the aforementioned CMRR problems while realizing a frequency response that is comparable to the neutralized differential pair considered in the preceding subsection. The emitter follower inputs eliminate Miller effect frequency response degradation, and in addition, their utilization in conjunction with transistors Q2 and Q3 allows for extraction of both single ended and differential outputs. Transistors Q2 and A3 operate as common base stage. The inductive nature of the input impedance of these stages serves to peak the common mode differential input impedance at high frequencies. The immediate result is that high frequency CMRR peaking is produced, while the low frequency CMRR is at least as acceptable as the CMRR evidenced in the circuit of Figure 2-10.

The approximate low-frequency small-signal model corresponding to the amplifier of Figure 2-11 is depicted in Figure 2-12. Transistors Q1 and Q4 are represented by common-collector hybrid parameter models, while the dynamic characteristics of devices Q2 and Q3 are simulated by common-base hybrid parameters. The open-circuit reverse voltage gain of Q1 and Q4 is taken to be unity, and both the open-circuit output conductance and reverse voltage gain of Q2 and Q4 are presumed to be zero. Similarly, the open circuit output conductance of Q1 and Q4 is ignored. It should be noted that

$$h_{ie} + (\beta_o + 1)h_{ib} \tag{2-43}$$

and

$$(1 - \alpha_o) = 1/(\beta_o + 1) \tag{2-44}$$

if all four active elements conduct identical emitter currents.

The application of KVL around the source circuit delivers

$$V_{S1} = R_S I_{S1} + \left[h_{ie} + (\beta_o + 1)(R_E + R_K)\right] I_1 - I_3 R_K \tag{2-45}$$

and

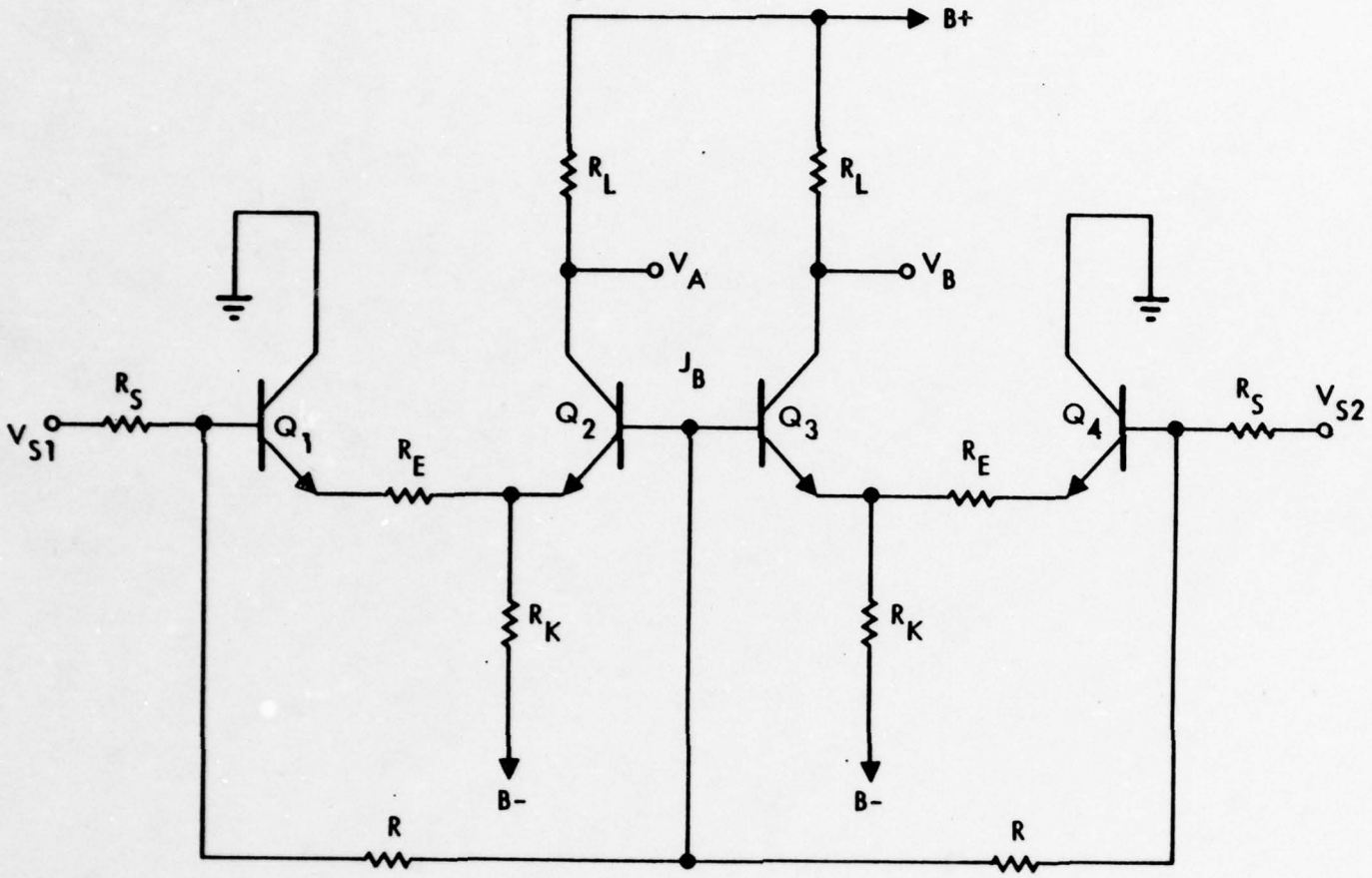


Figure 2-11 Simplified Schematic Diagram of Differential Quartet. Input signal voltages are V_{S1} and V_{S2}, while outputs are taken as V_A or V_B.

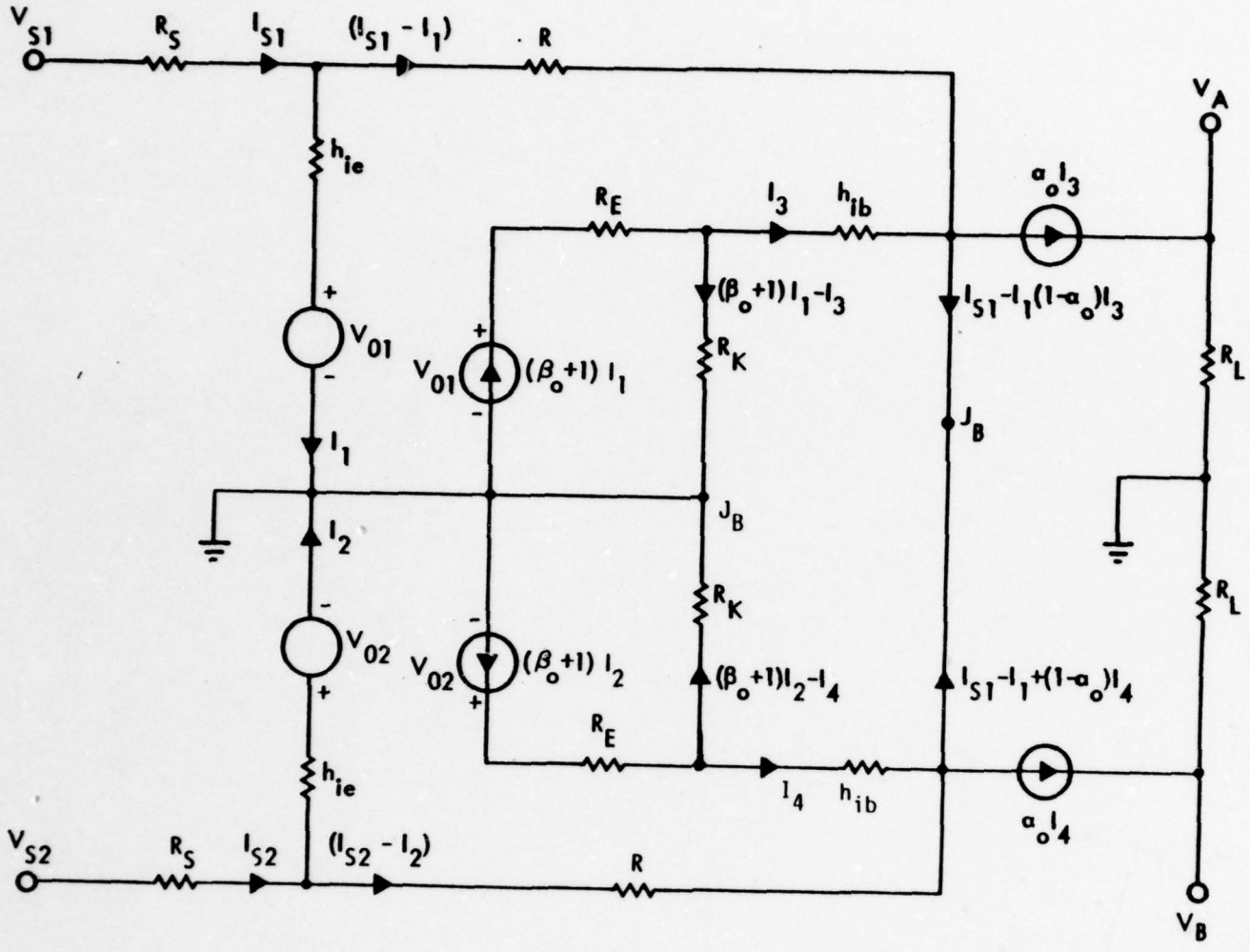


Figure 2-12 Approximate Low Frequency Small-Signal Model of Amplifier Given in Figure 2-11

$$V_{S2} = R_S I_{S2} + \left[h_{ie} + (\beta_o + 1)(R_E + R_K)\right] I_2 - I_4 R_K. \qquad (2\text{-}46)$$

Additionally,

$$(I_{S1} - I_1)R - h_{ib} I_3 - \left[h_{ie} + (\beta_o + 1)R_E\right] I_1 = 0 \qquad (2\text{-}47)$$

$$(I_{S2} - I_2)R - h_{ib} I_4 - \left[h_{ie} + (\beta_o + 1)R_E\right] I_2 = 0. \qquad (2\text{-}48)$$

Since currents at junction J_B (incidence node of the bases of Q2 and Q3) must sum to zero,

$$I_{S1} + I_{S2} = I_1 + I_2 - (I_3 + I_4)/(\beta_o + 1). \qquad (2\text{-}49)$$

Finally,

$$I_3 h_{ib} - I_4 h_{ib} + R_K \left[(\beta_o + 1)(I_2 - I_1) + I_3 - I_4\right] = 0, \qquad (2\text{-}50)$$

$$V_A = \alpha_o I_3 R_L \qquad (2\text{-}51)$$

$$V_B = \alpha_o I_4 R_L \,. \qquad (2\text{-}52)$$

Equations (2-45) through (2-50) can be solved for signal currents I_3 and I_4, and these solutions can be inserted into (2-51) and (2-52) to obtain the desired output voltage expressions. The pertinent results of the required algebraic manipulations are as follows:

$$(I_{S1} + I_{S2}) = - (I_3 + I_4) \left\{ \frac{R_E + 2h_{ib} + R/(\beta_o + 1)}{h_{ie} + (\beta_o + 1)R_E} \right\} ; \qquad (2\text{-}53)$$

$$(I_{S1} - I_{S2}) = \left\{ \frac{h_{ib}}{R} + \frac{(h_{ib} + R_K)\left[h_{ie} + R + (\beta_o + 1)R_E\right]}{(\beta_o + 1)R_K R} \right\} (I_3 - I_4); \qquad (2\text{-}54)$$

$$V_{S1} + V_{S2} = - R_C(I_3 + I_4); \tag{2-55}$$

$$V_{S1} - V_{S2} = R_D(I_3 - I_4). \tag{2-56}$$

In (2-55) and (2-56),

$$R_C = \left(h_{ib} + \frac{R}{\beta_o + 1}\right) + \left[\frac{R_K + R_S/\beta_o + 1}{R_E + h_{ib}}\right]\left[R_E + 2h_{ib} + \frac{R}{\beta_o + 1}\right] \tag{2-57}$$

and

$$R_D = R_E + h_{ib}\left(2 + \frac{h_{ib} + R_E}{R_K}\right) + \frac{R_S}{R}\left\{h_{ib} + \left(h_{ib} + R_E + \frac{R}{\beta_o + 1}\right)\left(1 + \frac{h_{ib}}{R_K}\right)\right\}. \tag{2-58}$$

For most practical purposes, $R_K >> R_S/(\beta_o + 1)$ and $R_K >> (R_E + h_{ib})$. Accordingly,

$$R_C \approx R_K\left\{1 + \frac{h_{ib} + R/(\beta_o + 1)}{h_{ib} + R_E}\right\} \tag{2-59}$$

$$R_D \approx R_E + 2h_{ib}. \tag{2-60}$$

In addition to the two approximations quoted above, (2-60) presumes $R_S << R$ and $(R_E + 2h_{ib}) >> R_S/(\beta_o + 1)$.

If (2-51) and (2-52) are combined with (2-55) and (2-56), it can be seen that

$$V_{S1} + V_{S2} = - \frac{R_C}{\alpha_o R_L}(V_A + V_B) \tag{2-61}$$

$$V_{S1} - V_{S2} = \frac{R_D}{\alpha_o R_L}(V_A - V_B). \tag{2-62}$$

These two relationships can be solved for either or both output voltages. The solution for V_A is

$$V_A = \frac{\alpha_o R_L}{2R_D}(V_{S1} - V_{S2}) - \frac{\alpha_o R_L}{2R_C}(V_{S1} + V_{S2}). \tag{2-63}$$

Now, observing that the differential input voltage is

$$V_D = V_{S1} - V_{S2} \tag{2-64}$$

and that the common mode excitation is

$$V_C = \frac{1}{2}(V_{S1} + V_{S2}), \tag{2-65}$$

(2-63) is meaningfully expressed as

$$V_A = A_D V_D + A_C V_C. \tag{2-66}$$

In (2-66), A_D and A_C, the differential mode and common mode voltage gains, respectively, are

$$A_D = \frac{\alpha_o R_L}{2R_D} \simeq \frac{\alpha_o R_L}{2(R_E + 2h_{ib})} \tag{2-67}$$

$$A_C = -\frac{\alpha_o R_L}{R_C} \simeq -\frac{\alpha_o R_L}{R_K}\left\{\frac{h_{ib} + R_E}{2h_{ib} + R_E + R/(\beta_o + 1)}\right\}. \tag{2-68}$$

It follows that the common mode rejection ratio (CMRR) is given by

$$\rho \triangleq \left|\frac{A_D}{A_C}\right| = \frac{R_C}{2R_D} \simeq \frac{R_K}{2(R_E + 2h_{ib})}\left\{1 + \frac{h_{ib} + R/(\beta_o + 1)}{h_{ib} + R_E}\right\} \tag{2-69}$$

An inspection of (2-68) and (2-69) clearly shows the need for large R_K if large CMRR is to be realized. Note, in particular, that R_C is directly proportional to R_K, while R_D is virtually independent of R_K.

Parameters R_C and R_D are closely related to the common mode and differential mode input resistances, respectively. For example, with $V_{S1} = V_{S2}$, which is symbolic of common mode excitation, (2-56) and (2-54) confirm $I_3 = I_4$ and $I_{S1} = I_{S2}$. Resultantly, (2-55) and (2-53) deliver

$$2V_{S1} = -2R_C I_3 = -R_C \left\{ \frac{h_{ie} + (\beta_o + 1)R_E}{R_E + 2h_{ib} + R/(\beta_o + 1)} \right\} (-2I_{S1}). \qquad (2\text{-}70)$$

The common mode input resistance, R_{inC}, is the ratio of V_{S1} to I_{S1}, under the condition of $V_{S1} = V_{S2}$. Using (2-70) and (2-59)

$$R_{inc} \simeq (\beta_o + 1)R_K. \qquad (2\text{-}71)$$

With $V_{S1} = -V_{S2}$, which is indicative of differential mode forcing, (2-55) shows that $I_4 = -I_3$, and (2-53) verifies $I_{S2} = -I_{S1}$. Then (2-56) and (2-54) give

$$2V_{S1} \simeq R_D \left\{ \frac{R}{R_E + 2h_{ib} + R/(\beta_o + 1)} \right\} (2I_{S1}). \qquad (2\text{-}72)$$

Using the last result and (2-60), it is easily shown that the differential mode input impedance, R_{inD}, is

$$R_{inD} \simeq R \| \left[(\beta_o + 1)(R_E + 2h_{ib}) \right] . \qquad (2\text{-}73)$$

The circuit of Figure 2-11 was subjected to a SPICE simulation.* No attempt was made to optimize gain, bandwidth, or power dissipation. Instead, interest was focused solely on the ability of the amplifier to maintain acceptable common mode response.

The differential mode, single-ended voltage gain, $V_B/(V_{S1} - V_{S2})$, is shown plotted as a function of frequency in Figure 2-13. As can be seen, the low frequency gain is almost 24dB, and the half-power bandwidth is approximately 110 MHz. Accordingly, the gain-bandwidth product is 1.7 GHz, which is about 40% of the operational short-circuit gain-bandwidth product of transistors Q2 and Q3. These two devices were made to operate at 4mA collector current and V_{CE} = 2.6 volts.

The common mode rejection ratio (CMRR) as a function of frequency is depicted in Figure 2-14. For the case of resistive coupling between the Q2 and Q3 emitters and B-, note that the CMRR is at least 20dB for all frequencies up to 500 MHz. Approximately 5dB of CMRR peaking is evident in the neighborhood of the 3dB differential mode bandwidth. This peaking is caused by the inductive nature of common base short circuit input impedance to which, as (2-69) verifies, the CMRR is functionally related.

* Inputs were capacitively coupled, and the bases of Q1 and Q4 were biased by an appropriate voltage divider network.

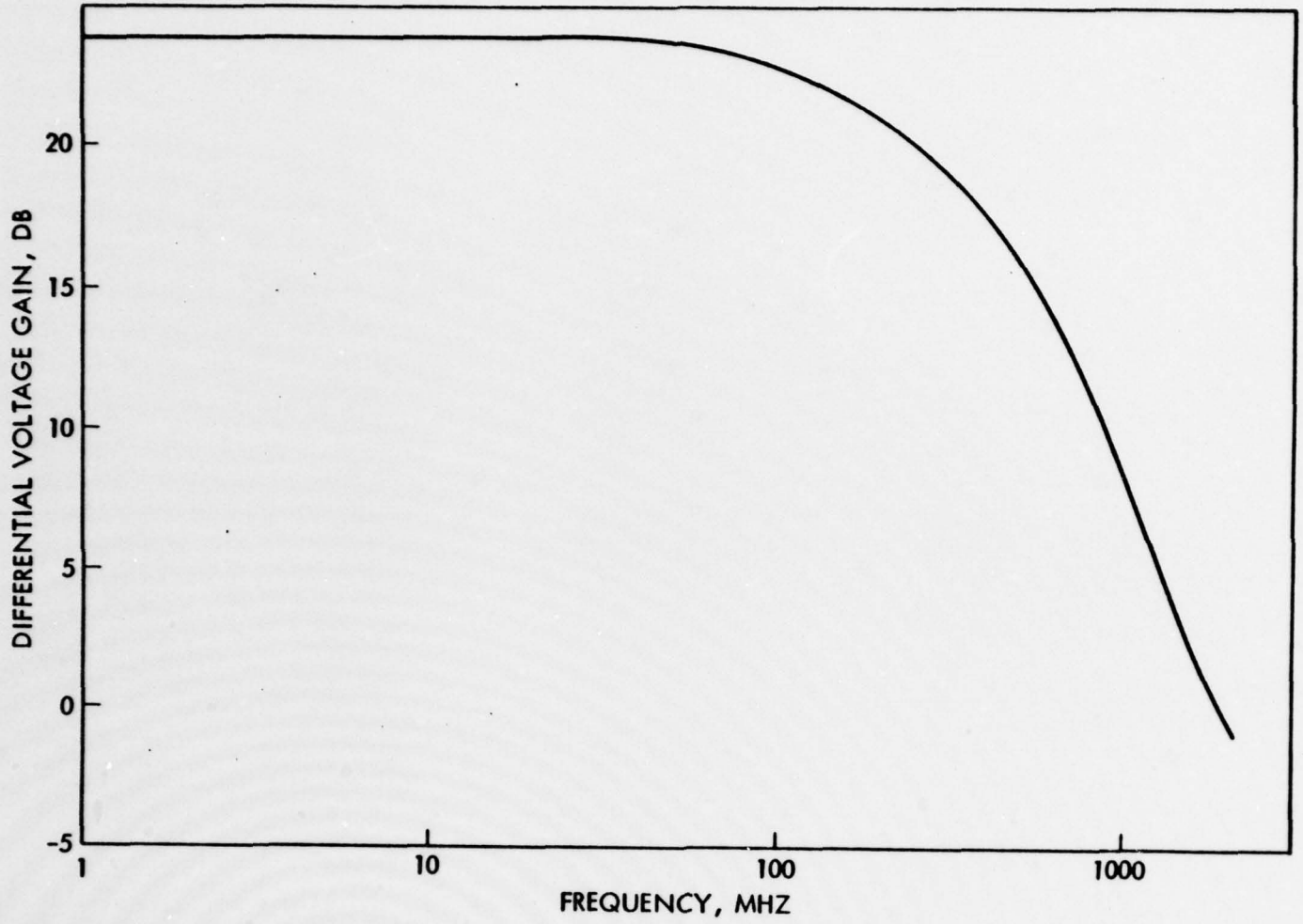


Figure 2-13 Differential Mode Gain, $V_B/(V_{S1} - V_{S2})$ for Circuit of Figure 2-11. Inputs are capacitively coupled and R_S = 50 ohms, R_L = 1500 ohms, R = 1000 ohms, R_K = 398 ohms, and R_E = 19.6 ohms.

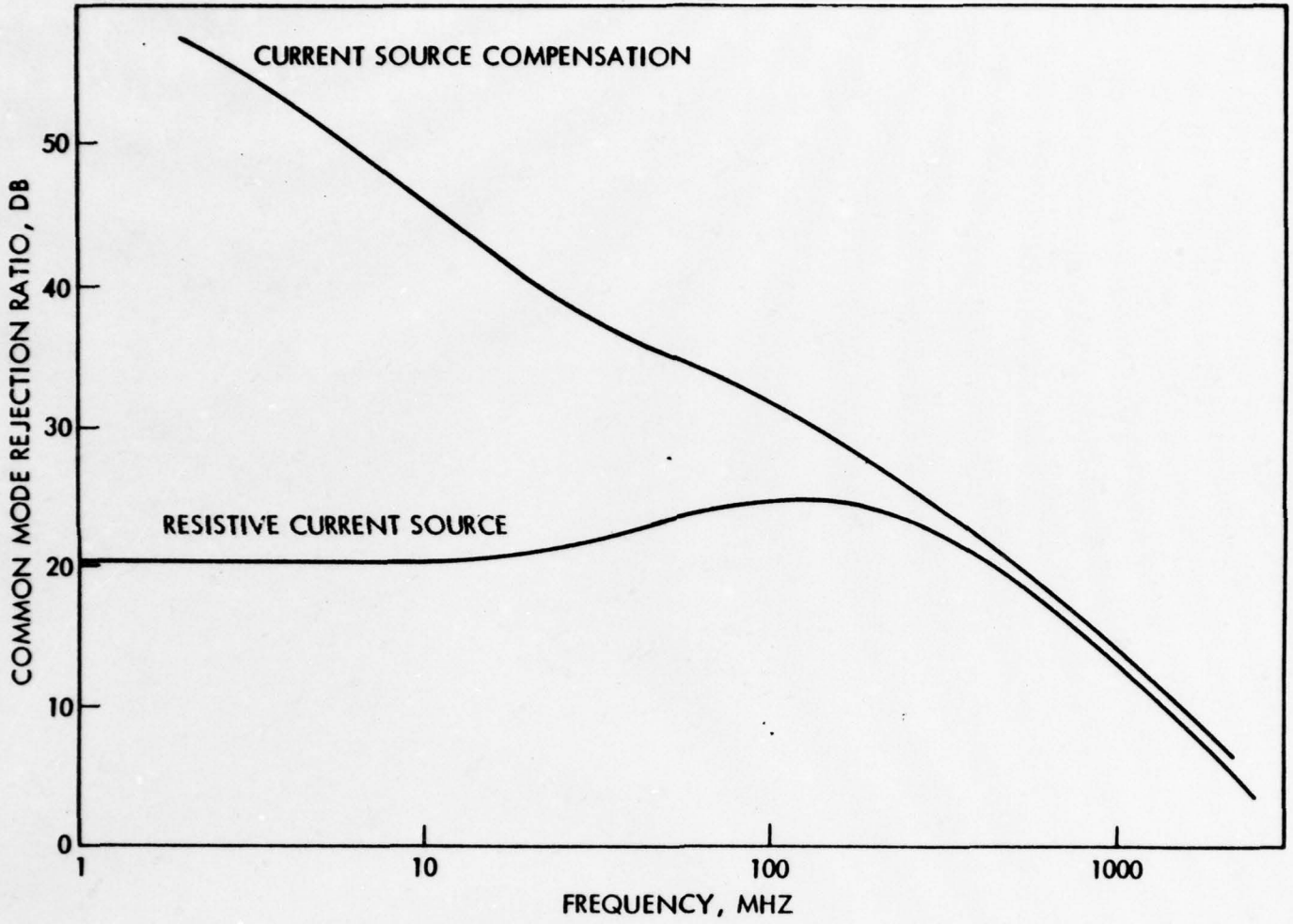


Figure 2-14 Common Mode Rejection Ratio as a Function of Frequency for Amplifier whose Voltage Gain is Depicted in Figure 2-13. Upper curve pertains to replacement of R_K in Figure 2-11 by conventional current source.

If R_K is replaced by a conventional current source, the CMRR is substantially enhanced at low frequencies. However, capacitive loading of the current source results in a high-frequency CMRR that is not substantially improved over its resistive current sink counterpart.

In an attempt to ascertain the common-mode effectiveness of the amplifier of Figure 2-11, the CMRR response of the traditional differential pair shown in Figure 2-15 was also simulated. Passive circuit elements were adjusted in this circuit to effect a low frequency CMRR that is identical to the CMRR evidenced at low frequencies by the circuit of Figure 2-11. The results displayed in Figure 2-16 clearly show that the compensated circuit displays superior CMRR at high frequencies.

2.1.6 Level Shifting

In the design of a monolithic linear amplifier, there is invariably a need for DC level shifting at amplifier interstages. This is to say that if interstages are to be direct coupled, the quiescent operating voltage of one stage is often too large to establish proper biasing of the subsequent stage. Accordingly, the need accrues for a circuit which supplies nominally constant gain over the frequency band of interest and moreover, operates at a quiescent output voltage which is appropriately downshifted from its quiescent input port voltage.

Historically, numerous level shifting circuits have been proposed. Among these are a variety of bridge configurations, diode junction voltage multipliers, and pn junction diode strings[3]. The latter two proposals are especially popular, since they make use of the base-emitter characteristics of MBJTs. Unfortunately, all of these networks suffer a degraded high frequency response. The zener diode is also a popular level shifter and although it offers an excellent frequency response, it suffers two disadvantages[4]. First, it is an electrically noisy device and second, its breakdown voltage is not a flexible parameter when it is synthesized in a sophisticated monolithic fabrication process; that is, its breakdown voltage cannot be specified by the designer but rather, it is dictated by design guidelines that must be invoked to ensure realization of other monolithic circuit performance measures.

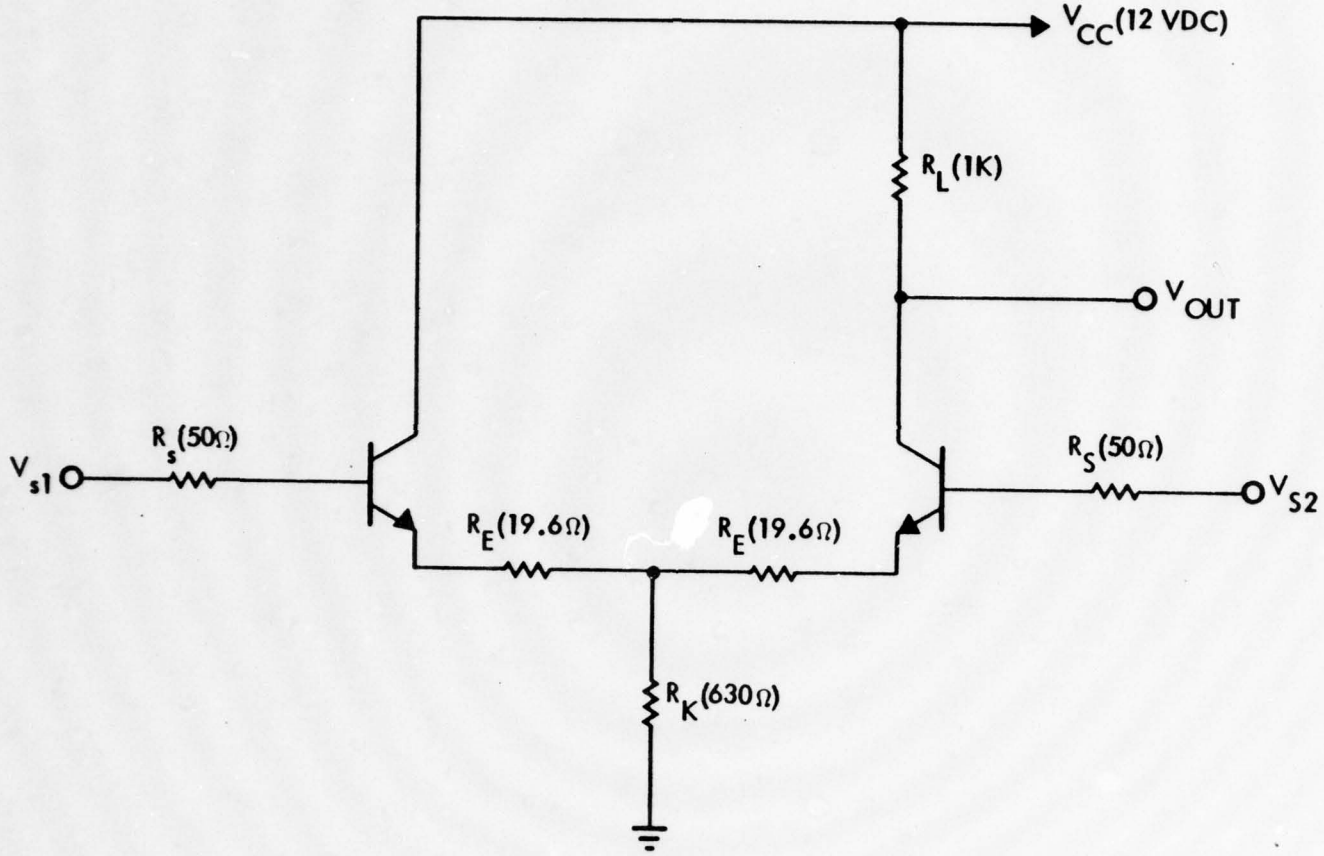


Figure 2-15 Simple Differential Pair.
Complete biasing network is not shown.

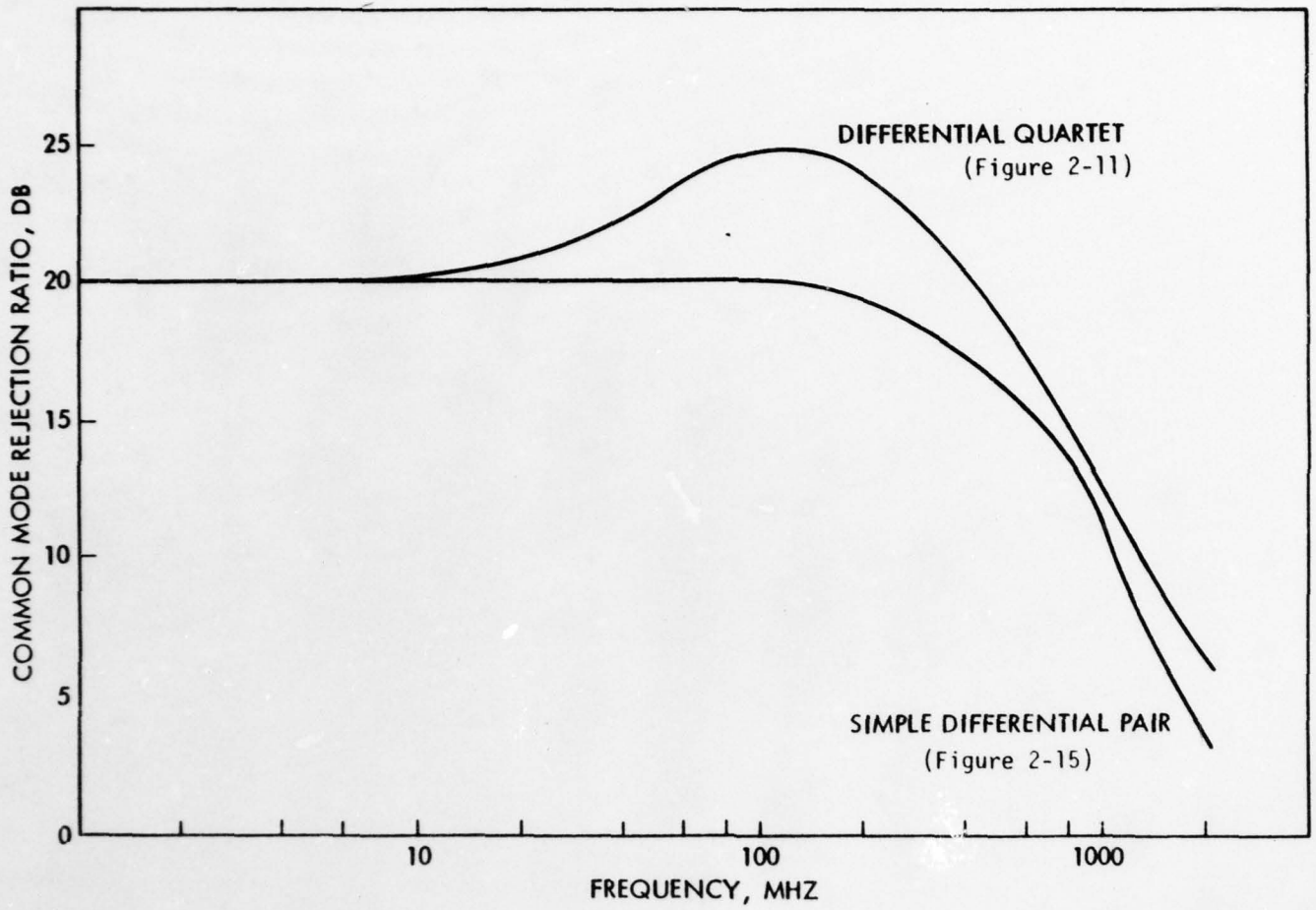


Figure 2-16 Common Mode Rejection Ratio Response of Simple Differential Amplifier and Differential Quartet

An alternative level shifting circuit is offered in Figure 2-17. The input signal is presumed to be superimposed with quiescent voltage, V_I, which is to be reduced to quiescent voltage V_S at the circuit output. Load Z_L represents the net output driving point impedance with which the level shift circuit interacts, while Z_S is the output impedance of the preceding stage. The circuit behaves as a multiplier of base-emitter junction voltage V_{BE} and utilizes Q2 as a source of controlled positive feedback to peak the high frequency response.

If transistors Q1 and Q2 are presumed to have identical static characteristics and if, in particular, R_B, R_E, and β_o respectively represent static values of intrinsic base resistance, intrinsic emitter resistance, and common emitter current transfer ratio, it can be shown that the amount of level shift is

$$V_I - V_S \simeq nV_{BE}. \tag{2-74}$$

In (2-74),

$$n \triangleq (2 + \frac{R_1}{R_2}) + \frac{Z_S + R_B + (\beta_o + 1)R_E}{(\beta_o + 1)R_2} \tag{2-75}$$

and the required approximations are

$$(\beta_o + 1) >> \frac{|R_1 + Z_S|}{nR_2}, \tag{2-76}$$

$$(\beta_o + 1 + \frac{Rin}{R_2}) >> \left|\frac{Rin + R_1 + Z_S}{Z_L}\right| , \tag{2-77}$$

where

$$Rin \triangleq R_B + (\beta_o + 1)R_E \tag{2-78}$$

is the input resistance seen at the base of either device. Observe that for large β_o, one can additionally approximate the base-emitter junction voltage multiplier in (2-75) by

$$n \simeq 2 + R_1/R_2. \tag{2-79}$$

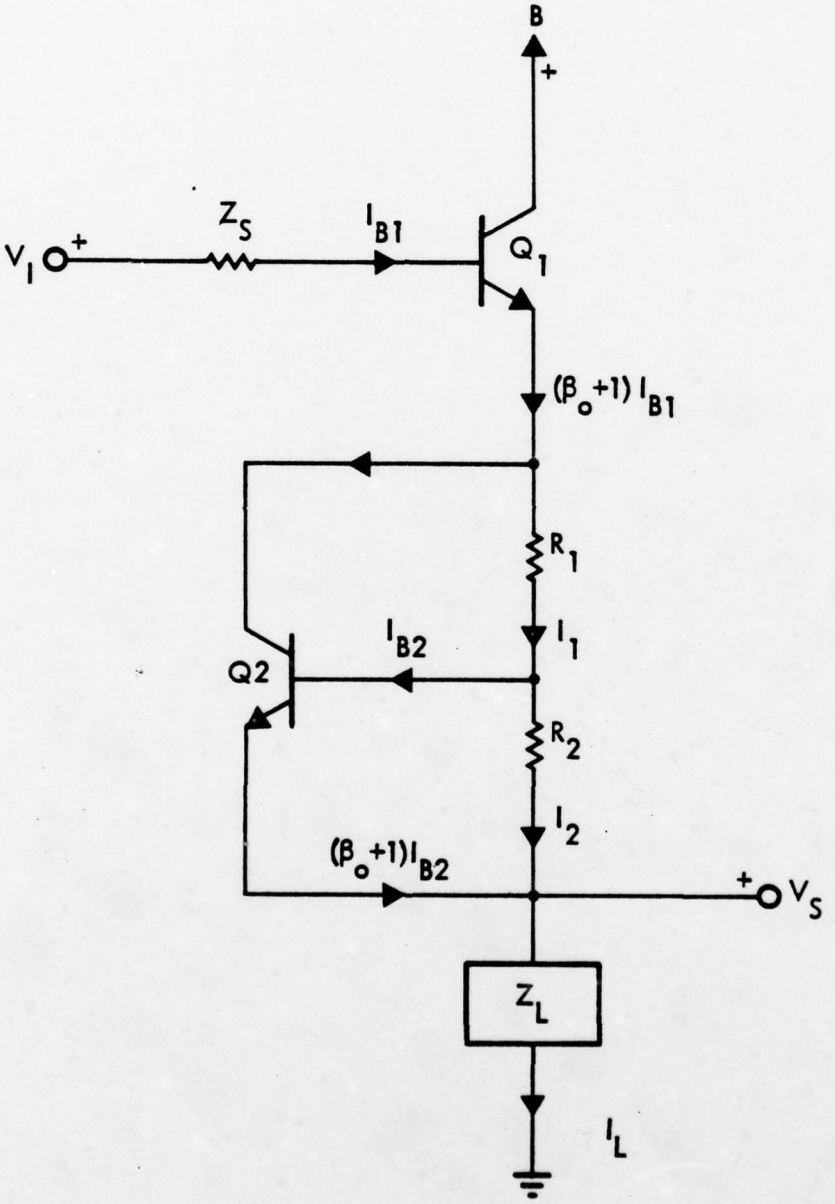


Figure 2-17 Proposed High Frequency Level Shifting Circuit

The circuit of Figure 2-17 was simulated on SPICE, with circuit parameter values as follows:

V_I = 5Vdc

Z_S = R_S = 140 ohms

R_1 = 1450 ohms

R_2 = 1200 ohms.

Additionally, load resistance (Z_L = R_L) was varied from 280 ohms-to-1200 ohms to ascertain the effect of transistor quiescent currents on small-signal response. Model parameters were extracted from measured scattering parameter data and adjusted to ensure conservative (pessimistic) simulation results.

The simulated frequency response is portrayed graphically is Figure 2-18. Clearly, the magnitude response improves dramatically with increasing DC load resistance. It is apparent that the current flowing through transistor Q2 is critical. An increasing Q2 collector current, coupled with a reasonably small base-collector bias magnitude, delivers a current gain that is too small to deliver adequately smooth frequency response. Table 2-1 lists current and gain as a function of load resistance.

TABLE 2-1 COLLECTOR CURRENT AND GAIN PARAMETERS FOR THREE LOAD RESISTANCES

Load Resistance (ohms)	Collector Current		Q2 Beta	
	Q1 (mA)	Q2 (ma)	(DC)	(AC)
280	7.7	7.0	41	29
500	4.8	4.1	49	38
1200	2.2	1.6	60	53

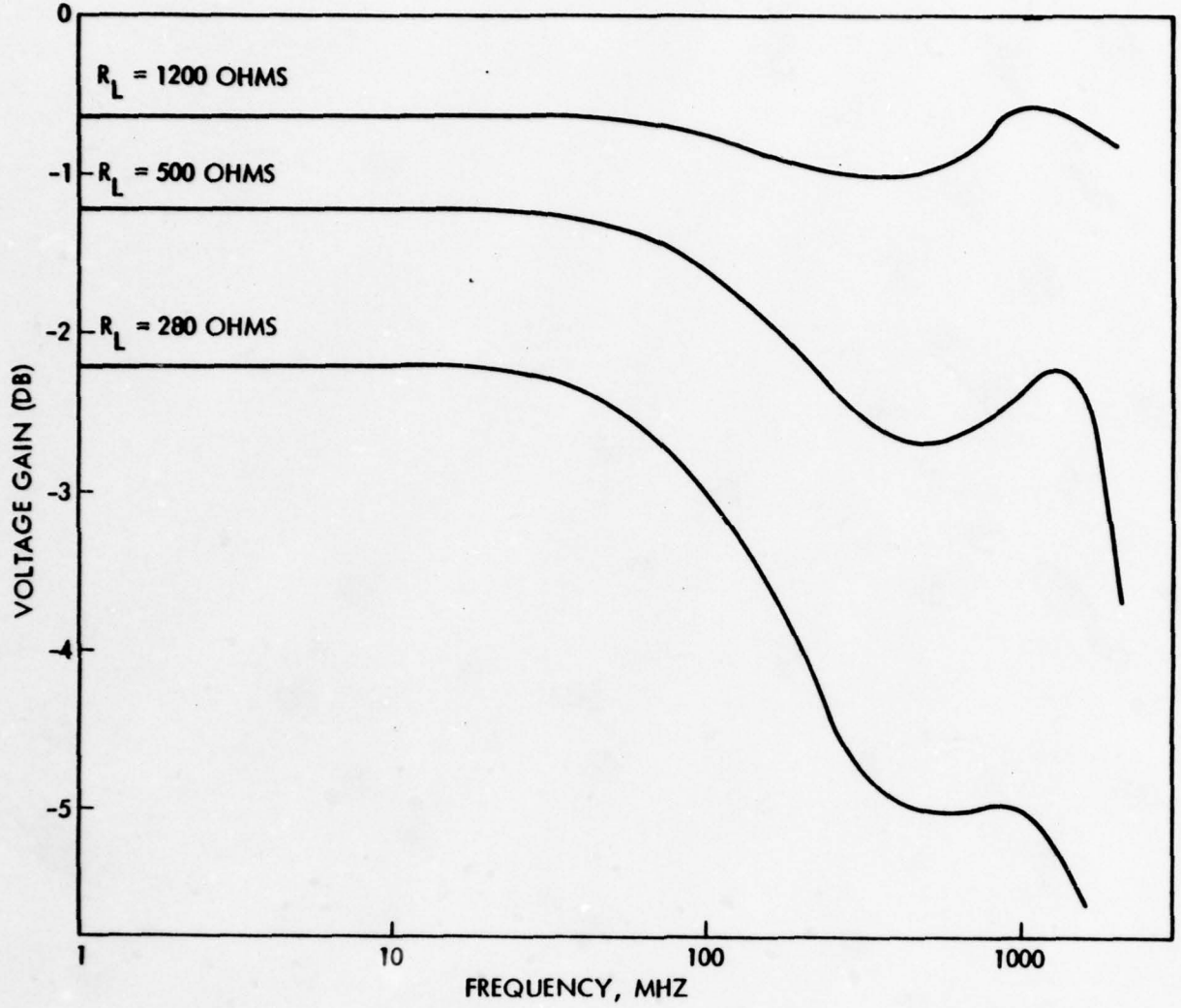


Figure 2-18 Frequency Response of Proposed Level Shifter

2.1.7 Thermal Stability

Very often, the satisfaction of a design specification mandates the need for a voltage source whose voltage is either temperature stabilized or is a linear function of a multiple of a semiconductor diode junction voltage drop. The situation in question is portrayed schematically in Figure 2-19 where under actual operating circumstances, the voltage developed across a load drawing I_L - amperes of current from the voltage source is

$$V_{OUT} = V_0 + KV_{BE}. \tag{2-80}$$

In (2-80), V_0 and constant K are ideally independent of temperature and active device parameters, while V_{BE} symbolizes the potential difference across a forward-biased semiconductor diode junction. A specific case in point is the circuit of Figure 2-3 where if beta for transistor QI is large and V_{II} is of the form, $V_0 + V_{BE}(K = 1)$, $V_0 = 2R_{EO}I_{EQ}$, thereby giving a transistor current that is ideally stablized with respect to temperature.

In the proposed supply voltage circuit of Figure 2-20, it is assumed that the transistors are identical and that the base-emitter junction voltages of each device are virtually the same. The equations relating emitter currents I and I_1 to power supply voltage V_{EE} are

$$V_{CC} = R_P\left\{I_1 + \frac{I}{\beta + 1} + \frac{V_{BE}}{R_2}\right\} + V_{BE} + (I - I_L)R_E - V_{EE} \tag{2-81}$$

and

$$0 = R_1\left\{\frac{I_1}{\beta + 1} + \frac{V_{BE}}{R_2}\right\} + R_S\left\{I_1 + \frac{V_{BE}}{R_2}\right\} - (I - I_L)R_E. \tag{2-82}$$

Equation (2-82) provides

$$I_1 = \left[\frac{R_E}{R_S + \frac{R_1}{\beta + 1}}\right](I - I_L) - \frac{\frac{R_1 + R_S}{R_2}V_{BE}}{R_S + \frac{R_1}{\beta + 1}}. \tag{2-83}$$

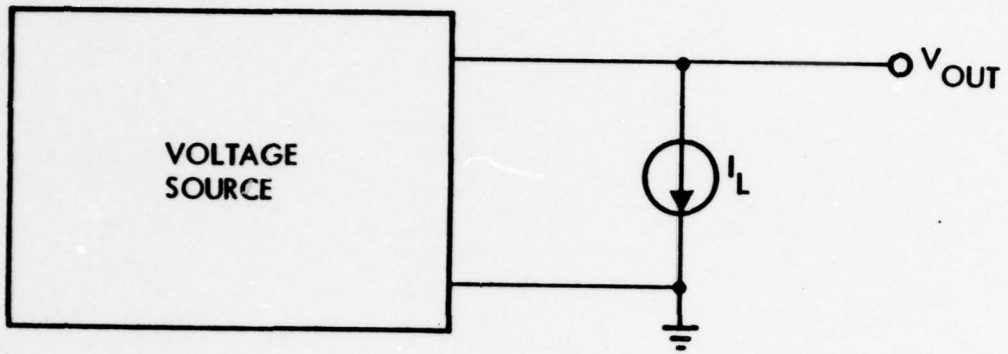


Figure 2-19 Schematic Diagram of Voltage Source. Under actual load conditions, $V_{OUT} = V_0 + KV_{BE}$, where V_0 and K are constants, independent of device parameters and temperature.

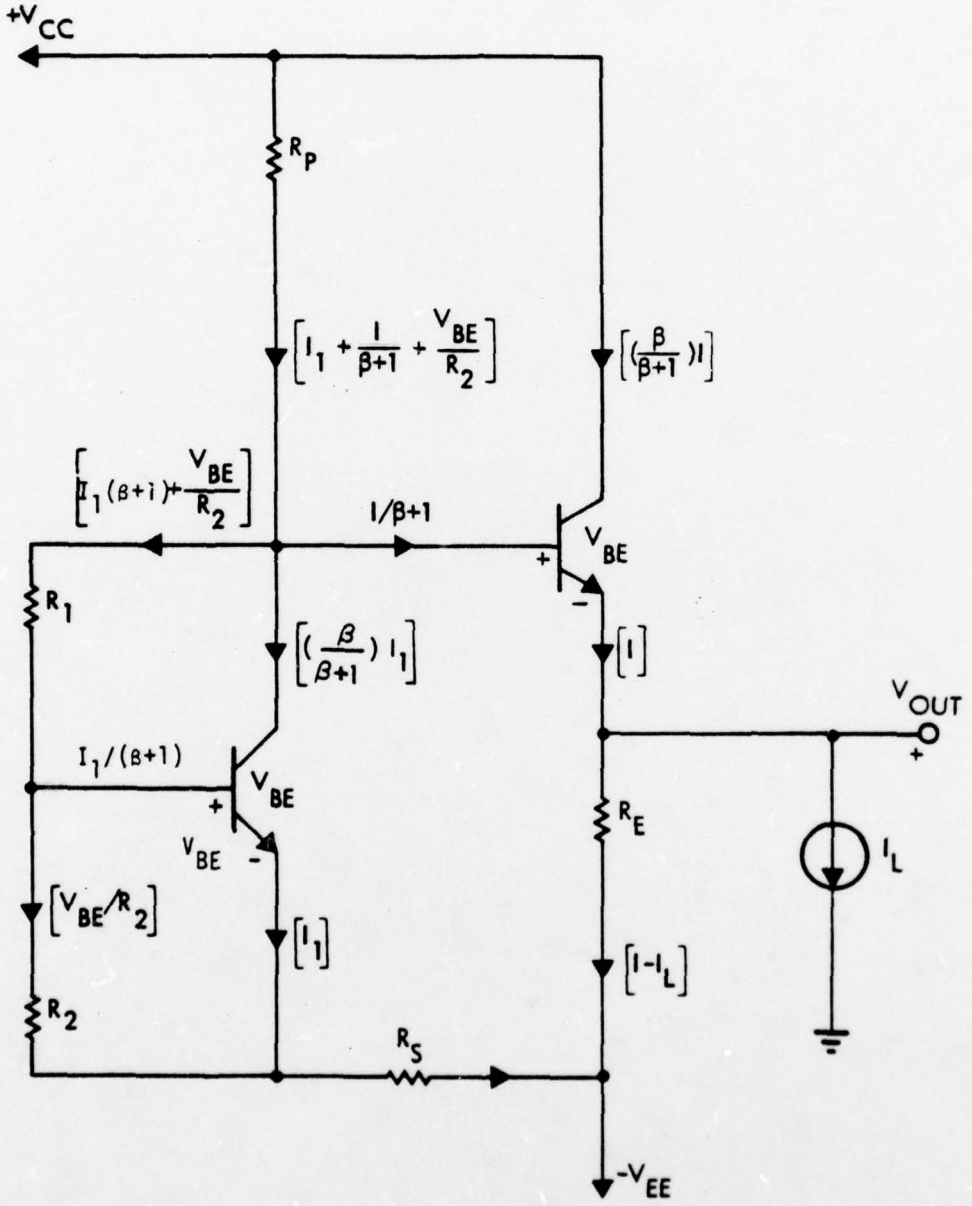


Figure 2-20 Proposed Circuit for Temperature-Stabilized Voltage Source

This result can be inserted into (2-81) and the resultant relationship solved for current I; accordingly;

$$I = \frac{V_{CC} + V_{EE} - V_{BE}\left\{1 + \frac{R_P}{R_2}\left[1 - \frac{R_1 + R_S}{R_S + R_1/(\beta + 1)}\right]\right\} + I_L R_E\left\{1 + \frac{R_P}{R_S + R_1/(\beta + 1)}\right\}}{R_E\left\{1 + \frac{R_P}{R_S + R_1/(\beta + 1)}\right\} + \frac{R_P}{\beta + 1}} \quad (2\text{-}84)$$

Since $V_{OUT} = (I - I_L)R_E - V_{EE}$, (2-84) yields,

$$V_{OUT} = -V_{EE}\left\{\frac{R_P\left[(1 - \alpha_o) + \frac{R_E}{R_S + (1 - \alpha_o)R_1}\right]}{R_E + R_P\left[(1 - \alpha_o) + \frac{R_E}{R_S + (1 - \alpha_o)R_1}\right]}\right\}$$

$$-I_L\left\{\frac{(1 - \alpha_o)R_P R_E}{R_E + R_P\left[(1 - \alpha_o) + \frac{R_E}{R_S + (1 - \alpha_o)R_1}\right]}\right\}$$

$$+ V_{CC}\left\{\frac{R_E}{R_E + R_P\left[(1 - \alpha_o) + \frac{R_E}{R_S + (1 - \alpha_o)R_1}\right]}\right\}$$

$$+ V_{BE}\left\{\frac{R_E}{R_E + R_P\left[(1 - \alpha_o) + \frac{R_E}{R_S + (1 - \alpha_o)R_1}\right]}\right\}\left[\left(\frac{\alpha_o R_P}{R_2}\right)\frac{R_1}{R_S + (1 - \alpha_o R_1} - 1\right], \quad (2\text{-}85)$$

where $\alpha_o = \beta/(\beta + 1)$ is the short circuit common base current transfer ratio.

A comparison of (2-85) with (2-80) leads to the conclusion that V_0 is the algebraic sum of the first three terms on the right hand side of (2-85). Moreover, if the last term in (2-85) is to represent a multiple, K, of V_{BE}, it is easy to establish that

$$\frac{\alpha_o R_1}{R_2} = \left[\frac{R_S + (1 - \alpha_o)R_1}{R_E}\right]\left[\frac{(1 + K)R_E}{R_P} + (1 - \alpha_o)K\right] + K. \quad (2\text{-}86)$$

Equation (2-86) simplifies to

$$\frac{\alpha_o R_1}{R_2} \simeq K + \frac{(1 + K)R_S}{R_P} \quad (2\text{-}87)$$

for

$$\left.\begin{aligned} R_1 &<< (\beta + 1)R_S \\ \frac{K}{1 + K} &<< \frac{(\beta + 1)R_E}{R_P} \end{aligned}\right\} \quad (2\text{-}88)$$

If, in addition to (2-88)

$$R_S << (\beta + 1)R_E, \quad (2\text{-}89)$$

(2-85) collapses to the form,

$$V_{OUT} = \left(\frac{R_S}{R_S + R_P}\right)V_{CC} - \left(\frac{R_P}{R_P + R_S}\right)\left[V_{EE} + \frac{R_S I_L}{\beta + 1}\right] + KV_{BE} \quad (2\text{-}90)$$

where it is understood that

$$V_0 = -\left(\frac{R_P}{R_P + R_S}\right)\left[V_{EE} + \frac{R_S}{\beta + 1}I_L\right] + \left(\frac{R_S}{R_S + R_P}\right)V_{CC}. \quad (2\text{-}91)$$

Observe that for large β and/or small load current, V_0 is virtually independent of device parameters and electrical characteristics. Note further that V_{OUT} in (2-90) is independent of resistance R_E, across which V_{OUT} in Figure 2-20 is developed.

2.2 Cascode Circuits

A cascode circuit is a compound interconnection of a common emitter transistor stage and a common base stage, as inferred by the simple AC schematic diagram of Figure 2-21. Two advantages are gleaned from cascode operation of transistor pairs. First, the low input resistance of the common base transistor, Q2, affords an effective input capacitance of transistor Q1 that is dramatically lower than the input capacitance realized if load resistance R_o is coupled directly into the collector of Q1 without benefit of the common base interstage. Second, the high frequency input impedance seen looking into the emitter of the common base transistor is invariably inductive over a wide range of load terminations. This inductance offers partial offset of the high frequency gain degradation incurred by the capacitive nature of common emitter output impedance. Indeed, as is shown subsequently, the inductance present at the emitter of either a common base or a common collector stage can be exploited to peak the frequency response in such a way as to realize optimal bandwidth or maximally flat magnitude of response.

2.2.1 Input Capacitance

Figure 2-22a depicts the single pole approximation to the high frequency small-signal equivalent circuit of a common emitter amplifier. The approximation is valid and provides a conservative bandwidth estimate if the actual poles of the amplifier are all real, the amplifier displays a dominant pole response in the vicinity of the 3dB bandwidth, and all actual amplifier zeros are real and sufficiently far removed from the dominant pole[5]. Parameters r_b, R_{pi}, g_m, and r_o are traditional hybrid parameters utilized in previous analyses, and R_L is the effective low frequency load resistance driven by the common emitter stage. It can be shown that [2],[6] the input capacitance at the base-emitter junction is

$$C_{in} = C_{TE} + (1 + g_m R_{L1})C_{TC} + \frac{R_{L1}C_{TC}}{R_{pi} \| (r_b + R_S)}, \qquad (2\text{-}92)$$

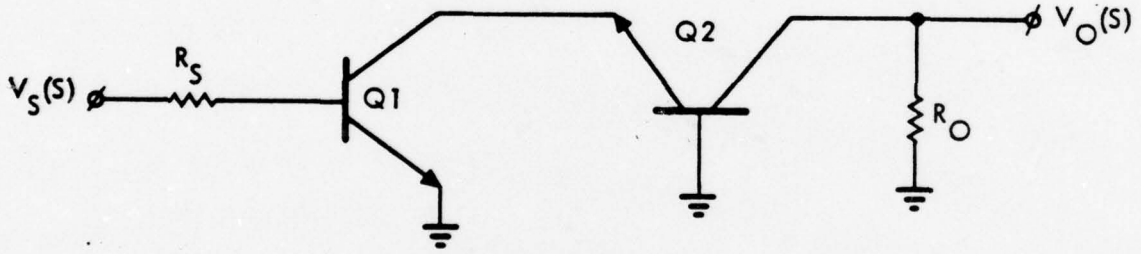
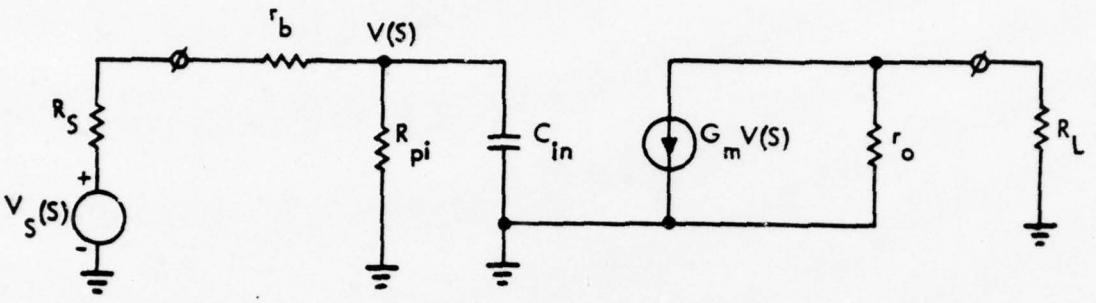
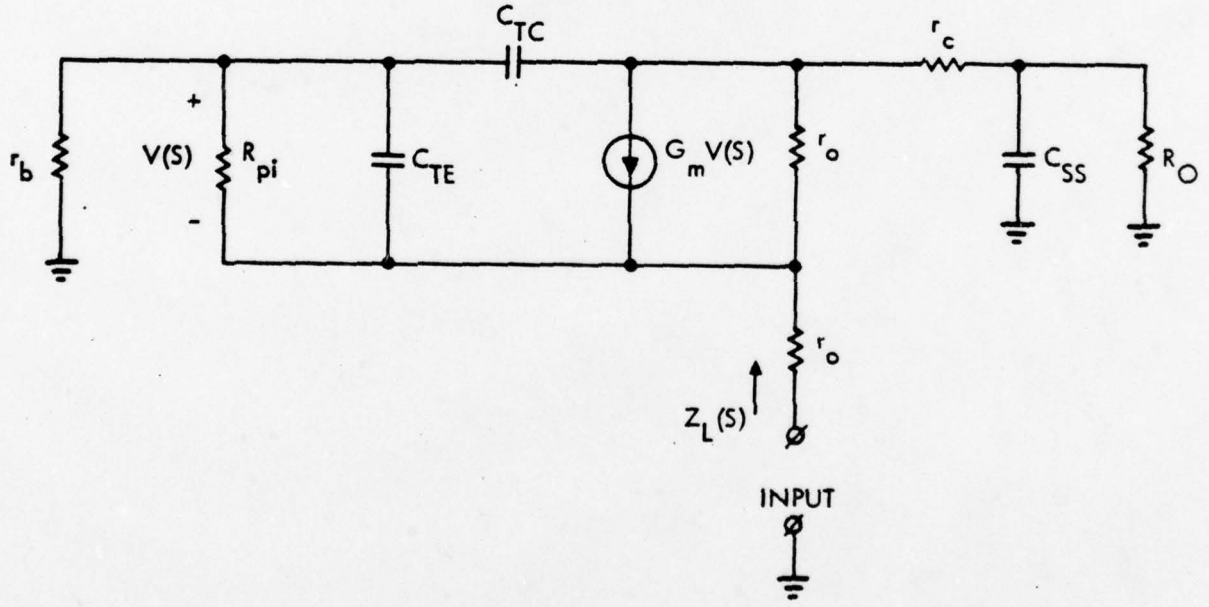


Figure 2-21 AC Schematic Diagram of Simple Cascode Amplifier



(a)



(b)

Figure 2-22 (a) Single Pole Approximation to Common Emitter High Frequency Equivalent Circuit.
(b) High Frequency Common Base Model.

where C_{TE} is the total capacitance at the base-emitter junction, C_{TC} is analogously defined for the base-collector junction, and R_{L1} is the net collector-emitter load at low frequencies. In most cases, $r_o >> R_L$ so that $R_{L1} \simeq R_L$.

The equivalent circuit for a common base stage appears in Figure 2-22b. The usual parameter definitions apply and additionally, r_e is the resistance of the emitter bulk, r_c is the resistance of the epitaxial layer, and C_{SS} represents substrate capacitance. By comparison of this circuit with the simplified schematic diagram of Figure 2-21, it can be seen that the low frequency value, say $Z_L(o)$, of impedance $Z_L(s)$ seen looking into the emitter is the net effective DC load presented to Q1 by Q2. A straight-forward low frequency analysis yields

$$Z_L(o) = \frac{R_{pi} + r_b}{\beta_o + 1} + r_e. \qquad (2\text{-}93)$$

The expression ignores the effects of r_o. From (2-92), the effective input capacitance of the cascode configuration is

$$C_{inc} = C_{TE} + (1 + g_m Z_{Lo})C_{TC} + \frac{Z_{Lo}C_{TC}}{R_{pi} \| (r_b + R_S)}, \qquad (2\text{-}94)$$

where r_o is once again tacitly ignored.

A numerical example may help to confirm the significance of cascoding. Let Q1 and Q2 be characterized by R_{pi} = 150 ohms, g_m = 300 mmhos, r_b = 65 ohms, $\beta_o = g_m R_{pi}$ = 45, C_{TE} = 15pF, C_{TC} = 0.30pF, r_e = 1.5 ohms, and r_o = 5000 ohms. Also, let the external terminations be R_o = 100 ohms and R_S = 50 ohms. Then if R_o directly loads the collector of Q1 in Figure 2-21, (2-92) gives for effective input capacitance,

$$C_{in} = 15 + (31)(0.3) + (1.506)(0.3) = 24.8\text{pF}.$$

On the other hand, if the common base unit is used, (2-93) gives $Z_L(o)$ = 6.2 ohms and by (2-94),

$$C_{inC} = 15 + (2.86)(0.3) + (0.095)(0.3) \simeq 15.9\text{pF}.$$

Thus, in this case, the input capacitance is reduced by almost 36%. Note that the contribution of C_{TC} is reduced by more than 90%!

Three points can be made at this juncture. First, the attenuation of input capacitance afforded by the common base stage is achieved without significant sacrifice in gain. This statement derives from the fact that the current gain of Q2 is only slightly less than unity, while small load resistances at the collector of Q1 afford a common emitter current gain magnitude that approaches β_o. Second, the single-ended configuration of Figure 2-21 is amenable to double-ended realization, as depicted in Figure 2-23. In this circuit, Q3 and Q4 are the common base components of the common emitter-common base cascode.

Finally, although the cascode system undeniably provides bandwidth expansion over a common emitter unit designed to supply comparable gain, the circuit is not without drawbacks. A more definitive high frequency analysis verifies that the common base portion of the cascode introduces two forward transmission poles. One of these poles is at $(-1/r_b C_{TE})$ and, owing to presumably small r_b, is significantly displaced from the dominant pole determined by C_{inC}. The other pole is located in the s-plane at $-1/(R_o + r_x)C_{TC}$. For large R_o, a state of affairs commensurate with the realization of large voltage gain, it is conceivable that the magnitude of this and the dominant pole can be virtually the same. Regardless, however, of the explicit nature of pole separation, it is clear that the additional poles are conducive to a rate of high frequency response roll-off which is faster than that evidenced in single stage common emitter orientation. This situation may prove troublesome when operation in the neighborhood of the band edge is required. Moreover, the excess phase lag associated with the additional poles are likely to cause stability problems if attempts are made to implement feedback around the entire cascode configuration.

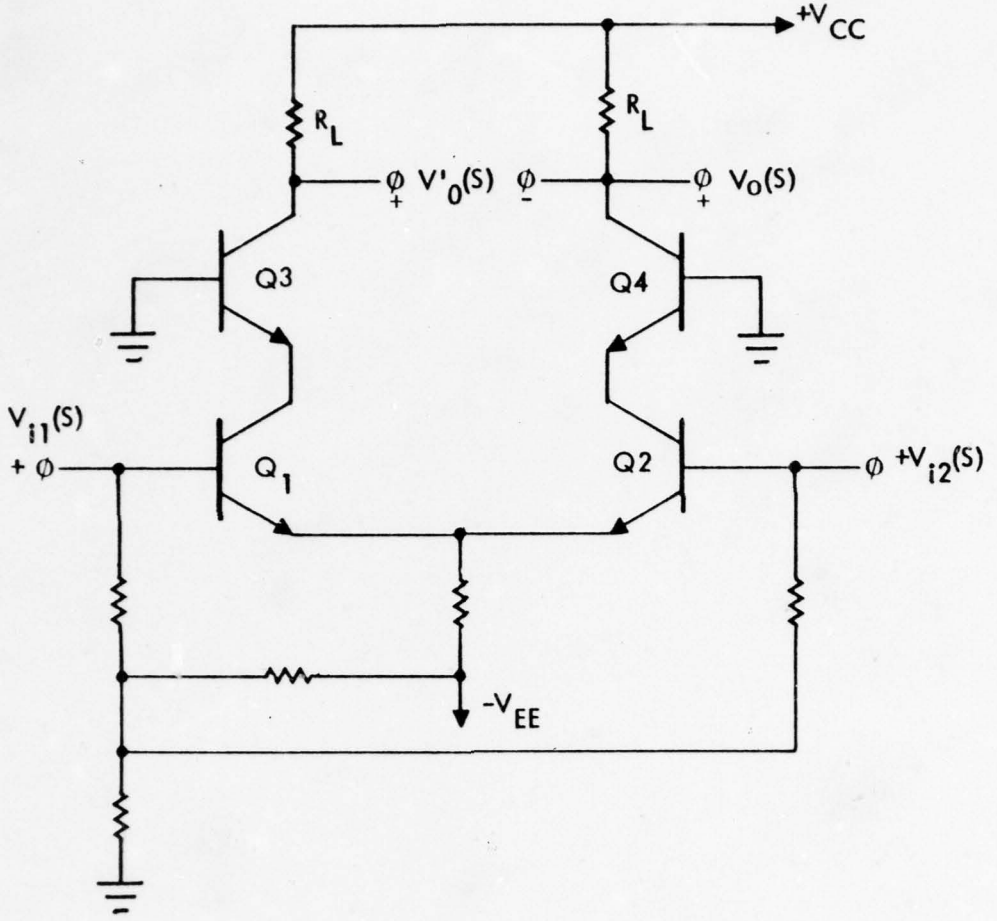


Figure 2-23 Differential Version of Cascode Circuit Shown in Figure 2-22. Unlabeled resistors are used for biasing.

2.2.2 Effective Emitter Inductance

The presence and ultimate broadband utility of the inductive nature of the impedance presented at the emitter of a common base or common collector stage has been alluded to in the preceding section of material. In order to exploit this effective inductance efficiently, it is necessary to understand its mathematical nature and concomittant design-oriented limitations.

The specific circuit addressed in this study is the grounded collector structure of Figure 2-24, wherein output impedance $Z_0(s)$ is to be determined. Figure 2-25 depicts the corresponding small-signal hybrid-pi model, in which intrinsic emitter resistance is absorbed by emitter resistance R_E, and in turn, this element is replaced by a one ampere current source so that the resultant emitter-to-ground voltage, $V_0(s)$, is numerically equivalent to $Z_0(s)$.

Nodal and loop analysis performed on the model of Figure 2-25 results in

$$V_0(s) = - \frac{1}{g_m + 1/R_{pi} + sC_{TE}} \tag{2-95}$$

and

$$r_c = V_0(s)\left\{1 + \frac{r_c + 1/sC_{TC}}{R_{BB}}\right\}$$

$$+ v\left\{1 + \frac{1}{sC_{TC}}(1/R_{pi} + sC_{TE}) + \frac{r_c + 1/sC_{TC}}{R_{BB}}\right\} . \tag{2-96}$$

Substitution of (2-95) into (2-96), followed by considerable algebraic manipulation, yields an expression of the form

$$Z_0(s) = R(s) + sL(s). \tag{2-97}$$

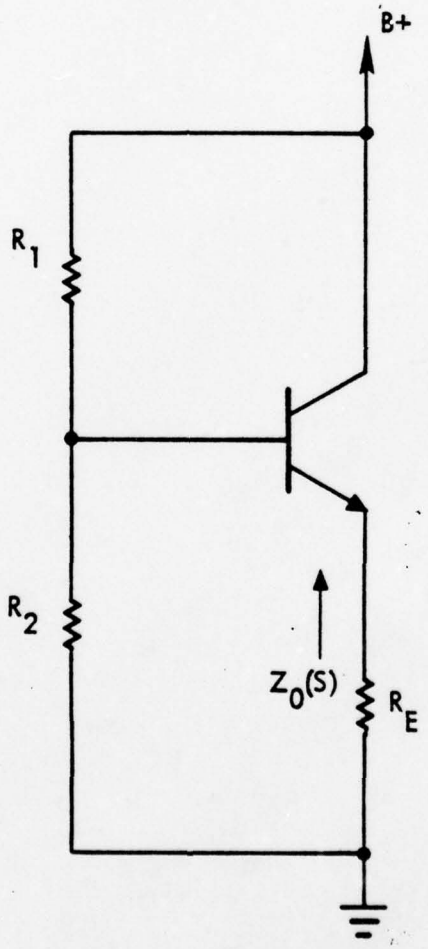


Figure 2-24 Emitter Follower Circuit

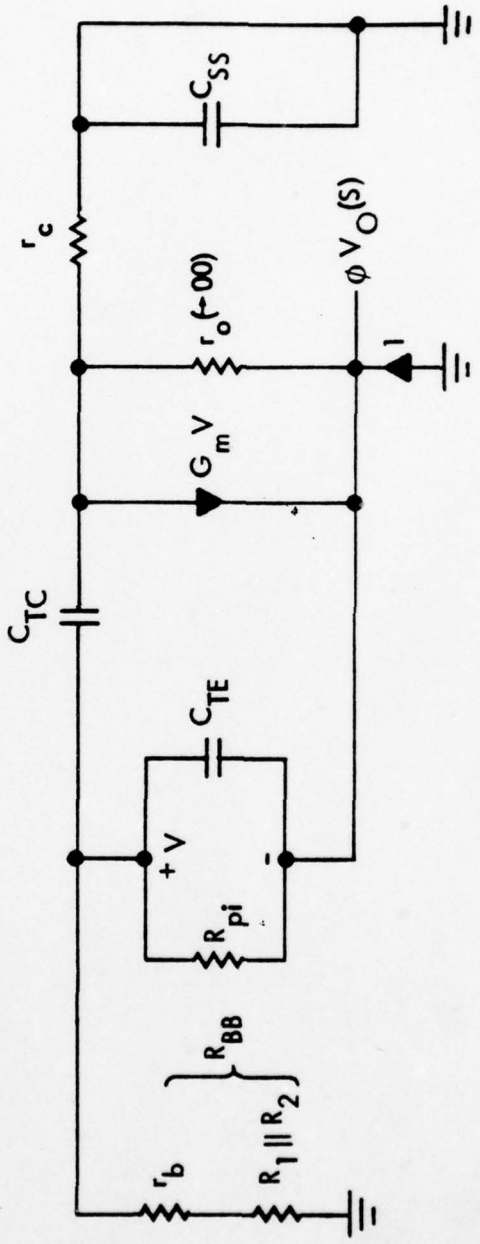


Figure 2-25 Small-Signal Model of Emitter Follower

In (2-97),

$$R(s) = \frac{R_{pi} + R_{BB}\left\{1 + \dfrac{s^2}{\omega_2\omega_\beta}\right\}}{(\beta_o + 1)(1 + s/\omega_1)(1 + s/\omega_T)} + r_e \qquad (2\text{-}98)$$

and

$$L(s) = \frac{(\dfrac{\omega_\beta + \omega_2}{\omega_2\omega_\beta})R_{BB} + \dfrac{R_{pi}}{\omega_1}\left\{1 + g_m(r_c \| R_{BB})\right\}}{(\beta_o + 1)(1 + s/\omega_1)(1 + s/\omega_T)} \qquad (2\text{-}99)$$

where

$$R_{BB} \triangleq r_b + R_1 \| R_2 \qquad (2\text{-}100)$$

is the net resistance in the base-ground loop, and

$$\beta_o \triangleq g_m R_{pi} \qquad (2\text{-}101)$$

is the approximate low frequency, short-circuit, common emitter current gain (AC beta) of the transistor. In arriving at (2-98) and (2-99) it is presumed that r_o is sufficiently large to justify its neglect. Finally,

$$\omega_\beta = 1/R_{pi}C_{TE} \ , \qquad (2\text{-}102)$$

$$\omega_T = (\beta_o + 1)\omega_\beta \ , \qquad (2\text{-}103)$$

$$\omega_1 = \frac{1}{(R_{BB} + r_C)C_{TC}} \ , \qquad (2\text{-}104)$$

and

$$\omega_2 = \frac{1}{r_C C_{TC}} \ . \qquad (2\text{-}105)$$

Note that for $C_{TE} >> C_{TC}$, ω_β is nominally the beta cutoff frequency of the device, while for $\beta_o >> 1$, f_T approximates the common emitter gain-bandwidth product.

It is reasonable to stipulate that $\omega_1 < \omega_T$, since for frequencies in excess of ω_T, the transistor ceases to function as a device capable of power gain. Thus, for $\omega < \omega_1$, and hence, $\omega < \omega_T$, the effective low frequency output inductance, assuming $\omega_1 << \omega_T$ is found from (2-99) as,

$$L_{EFF} \simeq \frac{r_c \| R_{BB}}{\omega_1} + \left(\frac{1}{\omega_2} + \frac{1}{\omega_\beta}\right)\frac{R_{BB}}{\beta_o + 1} + \frac{1}{g_m \omega_1}, \tag{2-106}$$

where use is made of the reasonable assumption, $\beta_o << 1$. The net inductance, L(s), is constant to within a factor of 0.707 of L_{EFF} up to frequency ω_1, which is given by (2-104). Note from (2-106) and (2-104) that

$$\omega_1 L_{EFF} = r_c \| R_{BB} + \frac{1}{g_m} + \omega_1 \left(\frac{1}{\omega_2} + \frac{1}{\omega_\beta}\right)\left(\frac{R_{BB}}{\beta_o + 1}\right). \tag{2-107}$$

For small intrinsic collector resistance, the first term on the right hand side of (2-107) is insignificant and, recalling (2-105), it is likely that $\omega_2 << \omega_\beta$. If large forward gain (g_m large) is additionally presumed, (2-107) reduces to

$$L_{EFF} \simeq \frac{R_{BB}}{\omega_T}, \tag{2-108}$$

where (2-103) is used. Equivalently, since r_c is assumed small in comparison with R_{BB}, (2-108) and (2-104) generate the result,

$$\omega_1 L_{EFF} \simeq \frac{1}{\omega_T C_{TC}}. \tag{2-109}$$

The preceding two results show that the inductance associated with the output impedance of a simple emitter follower is controllable by the net base-to-ground resistance. For a desired inductance value, the range of frequencies for which reasonably constant inductance is achievable is limited by the product of collector junction capacitance and transistor gain-bandwidth product.

It is important to point out that the quality factor of the effective low frequency inductance is fairly low. This assertion can be confirmed by noting in (2-98) that the low frequency resistance component of output impedance is

$$R(0) = r_e + \frac{R_{pi} + R_{BB}}{\beta_o + 1} \quad . \tag{2-110}$$

Thus, the quality factor of L_{EFF} at the highest frequency ω_1, of interest is

$$Q(\omega_1) = \frac{\omega_1 L_{EFF}}{R(0)} \simeq \frac{1}{\omega_T C_{TC}\left[r_e + \frac{1}{g_m} + \frac{R_{BB}}{\beta_o + 1}\right]} \quad . \tag{2-111}$$

As an example, for a 5 GHz device having C_{TC} = 0.5pF, g_m = 220 mmho, r_e = 2 ohms, β_o = 50, and R_{BB} = 1000 ohms at a given operating point, $Q(\omega_1)$ is only 2.4!

It is thus shown that the inductance associated with the output impedance of a simple emitter follower can be easily controlled by the net base resistance. Although the inductance is directly proportional to this resistance, R_{BB}, the frequency band over which constant inductance is attainable is inversely proportional to R_{BB}. Moreover, internal collector resistance also limits the frequency band in question.

2.2.3 Shunt-Peaked Amplifier

The existence of a designable inductance at the emitter-ground port of a common base or common collector amplifier suggest the possibility of an active realization of a shunt-peaked monolithic amplifier[7]. By "shunt peaking" is meant the introduction of an inductance in series with the load resistance of the amplifier. The purpose of the inductance is to achieve partial cancellation of a dominant pole established by the effective input capacitance of the succeeding stage. The situation in question is conceptually illustrated in Figure 2-26, wherein G_M symbolizes the forward transconductance of an amplifier driving load resistance R, C is the parasitic shunt output capacitance precipitated by subsequent circuitry, and L is the introduced peaking inductor.

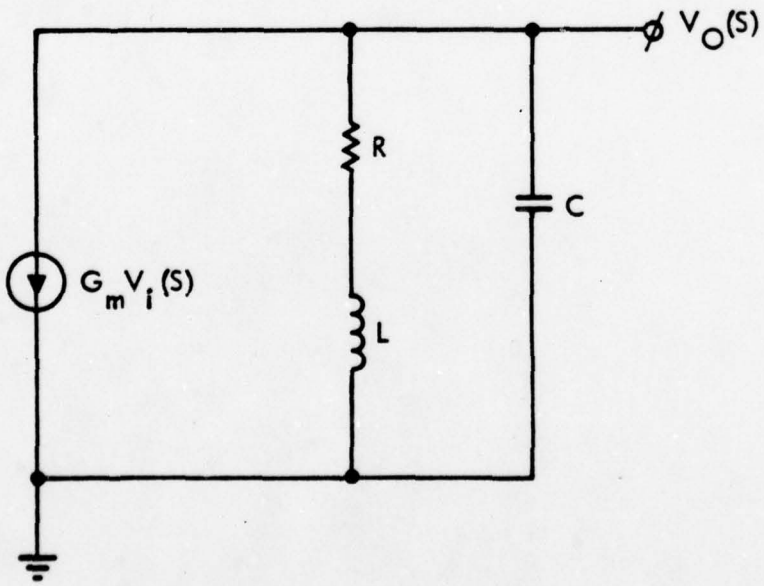


Figure 2-26 Simplified Model of Shunt-Peaked Interstage

For sinusoidal excitation, the steady state transfer function is

$$H(j\omega) = -G_M R\left\{\frac{1 + j\omega L/R}{1 - \omega^2 LC + j\omega RC}\right\} . \qquad (2\text{-}112)$$

Note that the zero frequency gain is $(-G_M R)$ and that with $L = 0$ (no peaking), the 3dB bandwidth is

$$B = \frac{1}{RC} . \qquad (2\text{-}113)$$

From (2-112), the gain normalized to $(-G_M R)$ is

$$H_N(j\omega) = \frac{1 + j\omega L/R}{1 - \omega^2 LC + j\omega RC} ,$$

whence

$$|H_N(j\omega)|^2 = \frac{1 + (\omega L/R)^2}{1 + \left[(RC)^2 - 2LC\right]\omega^2 + (LC)^2\omega^4} \qquad (2\text{-}114)$$

For a maximally flat magnitude (MFM) response, it is necessary to have[8]

$$\left(\frac{L}{R}\right)^2 = (RC)^2 - 2LC.$$

The positive inductance satisfying this constraint is

$$L = 0.4142R^2C = \frac{0.4142C}{B} , \qquad (2\text{-}115)$$

where B is understood to be the circuit bandwidth with $L = 0$. Substitution of (2-115) into (2-114) gives

$$|H_N(j\omega)|^2 = \frac{1 + 0.1716(\omega RC)^2}{1 + 0.1716(\omega RC)^2 + 0.1716(\omega RC)^4} \qquad (2\text{-}116)$$

The resultant 3dB bandwidth can be shown to be

$$B_L = 1.722B, \qquad (2\text{-}117)$$

which states that in theory, the effect of a peaking inductance optimized to the value set by (2-115) is to extend the non-peaked bandwidth by better than 72%.

Of course, 72% improvements in bandwidth are virtually unheard of in actual practice. Bandwidth enhancements of the order of 15%-to-25% are more believable and, in general, the factor by which shunt peaking can be expected to improve nominal circuit bandwidth dramatically decreases with progressively larger nominal bandwidths. This situation is a result of the fact that amplifiers possessed of extremely wideband frequency response capabilities tend to exude Gaussian, instead of dominant pole, frequency response characteristics[9]. That is, a single pole high frequency circuit model, such as that offered in Figure 2-26, constitutes extreme oversimplification of the analysis problem.

Nevertheless, shunt peaking can be profitably used in either single or double ended monolithic amplifiers. A representative differential, shunt-peaked cascode is provided in Figure 2-27. Transistors Q1 through Q4 comprise a common mode-compensated differential amplifier, while Q5 and Q6 are the common base components of an amplifier cascoded with Q2 and Q3. Finally, Q7 and Q8 realize the required inductance in accordance with the foregoing discussions.

2.3 Interstage Matching

The foregoing discussions address the problem of minimizing the effects of parasitic energy storances as a means of realizing wideband performance. Clearly, if energy storances can be completely eliminated, the amplifier undergoing design is transformed to an all-pass structure which, in theory, is capable of an infinitely broad pass-band. Needless to say, complete elimination of parasitic susceptances and reactances is unachievable over the entire spectrum of signal frequencies. However, the use of appropriately designed lossless interstage matching networks can eliminate the degrading effects of energy storances at a single frequency, and moreover, these matching networks can substantially reduce the rate of frequency response rolloff over a suprisingly broad range of signal frequencies[10].

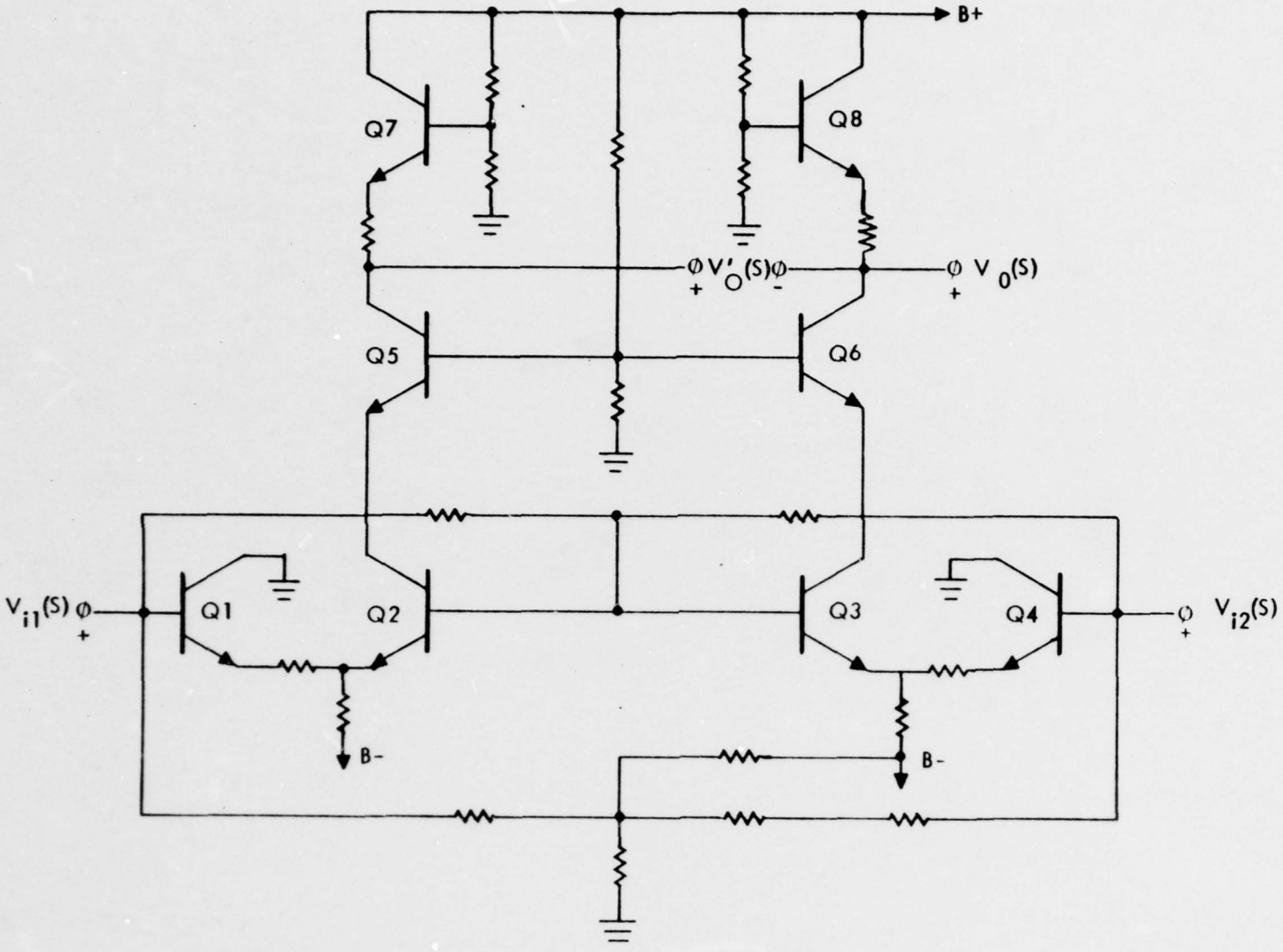


Figure 2-27 Differential Shunt-Peaked Cascode Amplifier

Figure 2-28a depicts the generalized situation. The output port of the first network is reduced to a simple output admittance in shunt with a voltage controlled current source, while the input port of the circuit driven by the first network is modeled as an input admittance. In general, one can suspect that transconductance G_M, the real parts of Y_{OUT} and Y_{IN}, and the imaginary parts of Y_{OUT} and Y_{IN} are all frequency variant. In particular, these parameters are well behaved functions of frequency and in the case of $R_e(Y_{OUT})$ and $R_e(Y_{IN})$, they are slowly varying functions of frequency. If C_1, C_2, and L are chosen such that

$$Y^*_{OUT}(j\omega) = Y_{IN}(j\omega), \tag{2-118}$$

where (*) symbolizes complex conjugation, the network driven by the controlled current source reduces to a pure conductance, $2G_{OUT}(\omega)$ as shown in Figure 2-28b. To the extent that G_{OUT} and G_M display nominally the same frequency dependence, voltage gain V_o/V_i is virtually frequency invariant, and broadbanded performance is realized. If the matching network is truly lossless, observe that the power delivered to the output port of Network #1 is the same as the power delivered to the input port of Network #2.

2.3.1 Matching Network Analysis

If $Y_{IN}(j\omega)$ is written

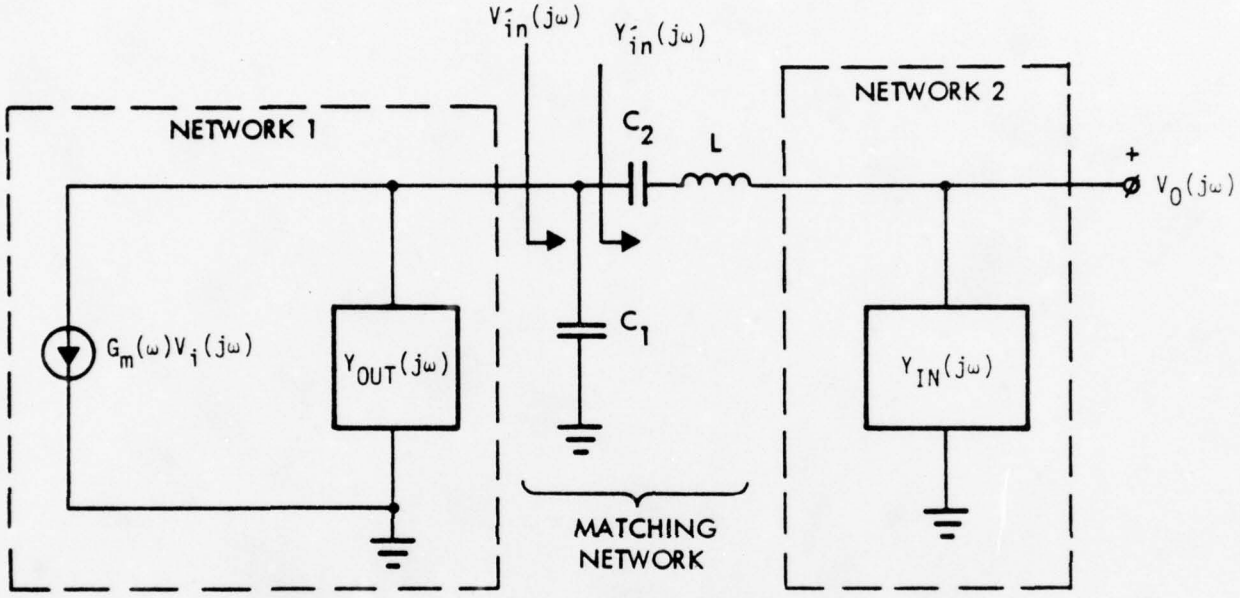
$$Y_{IN}(j\omega) = \frac{1}{R_{IN}(\omega)} + j\omega C_{IN}(\omega), \tag{2-119}$$

the impedance loading the Network #1 output port is

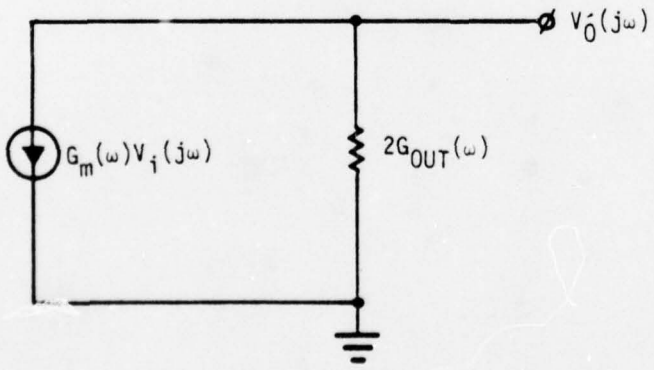
$$Z_{IN}(j\omega) = \frac{1}{Y_{IN}(j\omega)} = R_{IN}(\omega) + j\omega L_{IN}(\omega), \tag{2-120}$$

where

$$R_{IN}(\omega) = \frac{R_{IN}}{1 + (\omega R_{IN} C_{IN})^2}, \tag{2-121}$$



(a)



(b)

Figure 2-28 (a) Incorporation of Lossless Interstage Matching Network
(b) Equivalent Network if Matching Network Effects Conjugate Match Between $Y_{OUT}(j\omega)$ and $Y_{IN}(j\omega)$

$$\tilde{L_{IN}}(\omega) = L\left\{1 - \frac{1}{\omega^2 LC_2} - \left(\frac{\tilde{R_{IN}}(\omega)}{L}\right)R_{IN}C_{IN}\right\} . \qquad (2\text{-}122)$$

Then

$$\tilde{Y_{IN}}(j\omega) = j\omega C_1 + \tilde{Y_{IN}}(j\omega)$$

$$= \frac{\tilde{R_{IN}}}{(\tilde{R_{IN}})^2 + (\omega\tilde{L_{IN}})^2} + j\omega\left\{C_1 - \frac{\tilde{L_{IN}}}{(\tilde{R_{IN}})^2 + (\omega\tilde{L_{IN}})^2}\right\} . \qquad (2\text{-}123)$$

Now, if

$$Y_{OUT}(j\omega) \triangleq G_{OUT}(\omega) + j\omega C_{OUT}(\omega), \qquad (2\text{-}124)$$

the design requirements are

$$G_{OUT}(\omega) = \frac{\tilde{R_{IN}}(\omega)}{[\tilde{R_{IN}}(\omega)]^2 + [\tilde{L_{IN}}(\omega)]^2} , \qquad (2\text{-}125)$$

$$C_{OUT}(\omega) = \frac{\tilde{L_{IN}}(\omega)}{[\tilde{R_{IN}}(\omega)]^2 + [\tilde{L_{IN}}(\omega)]^2} - C_1. \qquad (2\text{-}126)$$

In practice, the procedural design steps are as follows. Given the input termination characteristics of Network #2 at frequency ω, $\tilde{R_{IN}}(\omega)$ is computed from (2-121). Then for stipulated G_{OUT} and C_{OUT} of Network #1 at the same frequency, ω, $\tilde{L_{IN}}(\omega)$ is found through use of (2-125), whence C_1 follows by (2-126). Capacitance C_2 is set equal to a factor of C_1, where the factor is determined from fabrication characteristics so that parasitics associated with monolithic capacitance realization are minimized. Then, L follows directly from (2-122).

A number of noteworthy comments can be offered at this point. First, it must be admitted that there is no guarantee that the values of C_1, C_2, and L commensurate with complex conjugate interstage matching are physically realizable. They may be too large to realize monolithically, they may be so small that inherent processing parasitics overshadow the primary intent of their utilization, or they may be non-positive. If one or more of these situations prevail, other matching networks must be found. Second, the proposed matching network, or multisection versions thereof, can also be used for delay equalization purposes, in addition to traditional impedance matching. This property is especially useful in the design of single-ended-to-differential amplifiers since, as previously shown, a mismatch in the relative phase response of the two outputs in a differential configurations causes deterioration in the common mode response. Finally, monolithic inductances are inherently plagued by low quality factor and parasitic distributed capacitances among the winding turns. This problem is definitively addressed in the next subsection.

2.3.2 Monolithic LC Impedance Characteristics

Figure 2-29 depicts a simplified schematic diagram of a monolithic LC network test pattern. Inductor L_o and C_o are chosen so that resonance is realized in the neighborhood of a frequency of 1 GHz. Resistance R_o establishes a finite quality factor (Q_o) for inductance L_o, and C/2 is a single lump approximation to the distributed susceptance associated with the coil. It should be pointed out that C_o and R_o can be measured in reasonably accurate fashion, but the accurate measurement of C (not C/2) constitutes a genuinely difficult problem.

The impedance, $Z_o(j\omega)$ between the terminals indicated in Figure 2-29, is

$$Z_o(j\omega) = \frac{1}{j\omega C_o} + \frac{R_o + j\omega L_o}{1 + j\omega R_o C/2 - \omega^2 L_o C/2}$$

$$= \frac{1 - \omega^2 L_o(C_o + \frac{C}{2}) + j\omega R_o(C_o + \frac{C}{2})}{j\omega C_o \left\{1 - \omega^2 L_o C/2 + j\omega R_o C/2\right\}} \quad . \qquad (2\text{-}127)$$

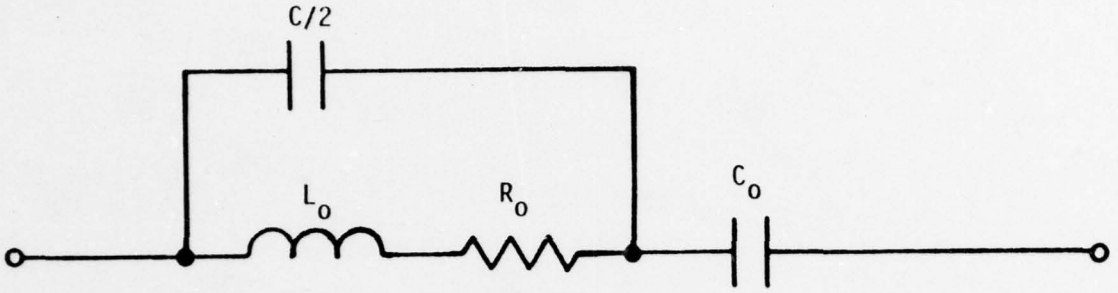


Figure 2-29 Simple Model of Fabricated Test Pattern

Letting

$$\omega_o = \frac{1}{\sqrt{L_o(C_o + \frac{C}{2})}} \quad , \tag{2-128}$$

$$\omega_p = \frac{1}{\sqrt{L_o C/2}} \quad , \tag{2-129}$$

$$Q_o = \frac{\omega_o L_o}{R_o} = \frac{1}{\omega_o R_o (C_o + \frac{C}{2})} \quad , \tag{2-130}$$

(2-127) can be shown to be equivalent to

$$Z_o(j\omega) = \frac{\frac{1}{Q_o \omega_o C_o} \left\{ 1 - \left(\frac{\omega}{\omega_p}\right)^2 - \left(\frac{\omega_o}{\omega_p}\right)^2 \left[1 - \left(\frac{\omega}{\omega_o}\right)^2 \right] \right\}}{\left[1 - \left(\frac{\omega}{\omega_p}\right)^2 \right]^2 + \left(\frac{\omega}{Q_o \omega_p}\right)^2 \left(\frac{\omega}{\omega_p}\right)^2}$$

$$+ j \left\{ \frac{\frac{\omega}{(Q_o \omega_p)^2 C_o} - \frac{1}{\omega C_o} \left[1 - \left(\frac{\omega}{\omega_o}\right)^2 \right] \left[1 - \left(\frac{\omega}{\omega_p}\right)^2 \right]}{\left[1 - \left(\frac{\omega}{\omega_p}\right)^2 \right]^2 + \left(\frac{\omega_o}{Q_o \omega_p}\right)^2 \left(\frac{\omega}{\omega_p}\right)^2} \right\} \quad . \tag{2-131}$$

In (2-128) through (2-131), ω_p is a parasitic frequency of resonance between the fabricated inductance and distributed capacitance. If ω_p is very large, which is indicative of very small distributed capacitance, ω_o is very nearly given by the idealized design value, $1/\sqrt{L_o C_o}$. In particular, note from (2-128) and (2-129) that

$$\omega_o = \frac{\omega_p}{\sqrt{1 + \omega_p^2 L_o C_o}} \quad , \tag{2-132}$$

which reduces to the ideal result if $\omega_p^2 L_o C_o >> 1$. Parameter Q_o in (2-130) represents the effective coil quality factor at radial frequency ω_o. Finally, observe that for $\omega_p \to \infty$ ($C \to 0$), (2-131) reduces to the expected result,

$$Z_o(j\omega) = \frac{1}{Q_o \omega_o C_o} - j\frac{1}{\omega C_o} + j\frac{\omega}{\omega_o^2 C_o} = R_o + \frac{1}{j\omega C_o} + j\omega L_o. \qquad (2\text{-}133)$$

The actual resonant frequency, say ω_x, is the frequency at which the imaginary component of $Z_o(j\omega)$ vanishes. From (2-131), ω_x must satisfy the requirement,

$$\left[1 - \left(\frac{\omega_x}{\omega_o}\right)^2\right]\left[1 - \left(\frac{\omega_x}{\omega_p}\right)^2\right] + \left(\frac{\omega_x}{Q_o \omega_p}\right)^2 = 0. \qquad (2\text{-}134)$$

The positive roots of this equation are $\omega_x \approx \omega_o$ and $\omega_x \approx \omega_p$, provided $Q_o^2 >> 1$. This is to say that (2-128) and (2-129) are approximately the two resonant frequencies displayed by the LC test circuit of Figure 2-29. In practice it is found that for $Q \geq 2$, the errors between the approximate roots, ω_o and ω_p, and the exact roots of (2-134) are less than 5%.

The simplest conceptual model for the circuit of Figure 2-29 is the series RLC structure shown in Figure 2-30. In this model, all three elements are frequency variant, and it might be stated that the sensitivity of these elements to frequency is a measure of the degree by which the parasitic capacitance, C, influences the terminal characteristics of an idealized RLC structure.

Recalling (2-131), the problem is to determine $R_s(\omega)$, $L_s(\omega)$, and $C_s(\omega)$ such that

$$Z_o(j\omega) = R_s(\omega) + j\omega L_s(\omega) + \frac{1}{j\omega C_s(\omega)} \qquad (2\text{-}135)$$

where it is understood that $R_s(\omega)$, $L_s(\omega)$ and $C_s(\omega)$ are positive real functions of frequency. If

$$D(\omega) \triangleq \left[1 - \left(\frac{\omega}{\omega_p}\right)^2\right]^2 + \left(\frac{\omega_o}{Q_o \omega_p}\right)^2 \left(\frac{\omega}{\omega_p}\right)^2, \qquad (2\text{-}136)$$

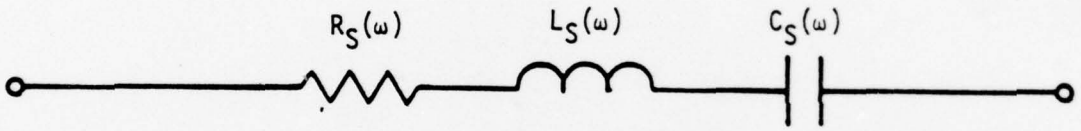


Figure 2-30 The Series RLC Equivalent Structure for the Model of Figure 2-29

it is clear that

$$Q_o\omega_o C_o R_s(\omega) = \frac{1 - \left(\frac{\omega_o}{\omega_p}\right)^2}{D(\omega)} . \tag{2-137}$$

Furthermore, it is easily verified that

$$\omega_o{}^2 C_o L_s(\omega) = \frac{1 + \left(\frac{\omega_o}{\omega_p}\right)^2 + \left(\frac{\omega_o}{Q_o\omega_p}\right)^2}{D(\omega)} , \tag{2-138}$$

$$\frac{C_s(\omega)}{C_o} = \frac{D(\omega)}{1 + \left(\frac{\omega^2}{\omega_o\omega_p}\right)^2} . \tag{2-139}$$

From the last two expressions,

$$\omega_o{}^2 L_s(\omega) C_s(\omega) = \frac{1 + \left(\frac{\omega_o}{\omega_p}\right)^2 + \left(\frac{\omega_o}{Q_o\omega_p}\right)^2}{1 + \left(\frac{\omega^2}{\omega_o\omega_p}\right)^2} , \tag{2-140}$$

which shows that $\omega_o{}^2 L_s(\omega) C_s(\omega)$ is a constant for all input signal frequencies that satisfy

$$\left(\frac{\omega^2}{\omega_o\omega_p}\right)^2 << 1. \tag{2-141}$$

In equality (2-141) is satisfied to within one part in 10 if

$$\omega \leq 0.56\sqrt{\omega_o\omega_p} \triangleq \omega_L . \tag{2-142}$$

If (2-142) is satisfied for all input signal frequencies of interest, the model of Figure 2-30 is meaningful in the sense that the product of effective inductance and effective capacitance determines the lowest resonant frequency of the LC test pattern. This is to say that satisfaction of (2-142) ensures that $L_s(\omega)$ and $C_s(\omega)$ in Figure 2-30 behave in much the same fashion as do frequency-invariant L and C in a conventional RLC circuit. More importantly, (2-142) establishes a practical frequency limit to a fabricated LC test circuit since for $\omega > \omega_L$, the required model is much to complicated to expedite a design procedure which ensures reliable and repeatable LC circuit fabrication.

The scattering parameters were measured for numerous types of LC test patterns over the frequency range of 100-to-2000 MHz. The results presented herewith pertain to the three types of patterns that most closely emulate the LC structures utilized in the GPS chip.

Approximately one dozen samples of each of three types of patterns were experimentally characterized. The measured s-parameters of each sample were inputed into COMPACT for the purpose of ascertaining optimal values of resistance, inductance, and capacitance in a simple series RLC configuration of the form shown in Figure 2-30. In effect, COMPACT was used to supplant the frequency variant elements in the model of Figure 2-30 with constant linear circuit elements that provided an acceptable match of experimental and theoretical response over the quoted frequency range. The subsequently presented tabularized results are averages for all samples studied; a standard deviation, in percent of the associated mean, is also presented.

The averaged optimized RLC parameters were then utilized to simulate the response of the circuit of Figure 2-30 on SPICE. The simulated value of resonant frequency was compared to the experimental value, the latter being discerned by examining the impedance computed directly from measured s-parameters. In all three cases, simulated and experimental values of resonant frequency agreed to within an error of no more than 5%.

The value of the parasitic capacitance, C/2, was estimated by assuming that the optimized capacitance is $(C_o + C/2)$. Capacitance C_o was computed from known processing characteristics and then, C_o was subtracted from the optimal capacitance value to identify capacitance C/2.

In an attempt to lend further credence to the foregoing experimental results, both the static resistance, R_o, and the series capacitance, C_o, were measured by directly probing the appropriate nodes in the circuit of Figure 2-29. The measured and optimized values of these circuit elements were found to agree in all cases to within a maximum error of approximately 12%.

The rather disconcerting conclusion that must be drawn is that the fabricated value of inductance is markedly lower than expected or computed inductance values. Two points are of interest. First, the fabricated inductance value is lower than the anticipated inductance by about the same factor in all cases examined. For Device #1, the factor is 2.45, for Device #2, it is 2.58, and for Device #3, the factor is 2.55. Second, the resultant resonant frequency is higher than anticipated by an average factor of 1.4. This enhancement can be somewhat explained by the lower inductance values that are ostensibly realized. The bottom line is that assuming an adequate experimental procedure, the number of turns and/or the associated area of inductances utilized in the GPS chip must be increased to offset the aforementioned inductance anomalies.

Finally, it should be noted that Device #2 offers the best approximation to an idealized series RLC structure, in the sense that the useable frequency range of a simple series RLC model on the LC test pattern is largest for this device. Observe, in addition, that Device #3 has the smallest such useable frequency range.

TABLE 2-2 OPTIMIZED PARAMETERS FOR DEVICE #1
(Line Width = 0.25 mil, Line Spacing = 0.25 mil, 7 turns)

OPTIMIZED INDUCTANCE	8.6130 nhy $\pm$ 3.35%	= $L(\omega)$
EXPECTED INDUCTANCE:	21.06 nhy	
OPTIMIZED RESISTANCE:	35.237 ohms $\pm$ 8.87%	= $R(\omega)$
EXPECTED RESISTANCE:	28 ohms	
OPTIMIZED CAPACITANCE:	1.6823 pF $\pm$ 2.56%	= $C(\omega)$
ESTIMATED PARASITIC:	0.535 pF	= C/2
RESONANT FREQUENCY:	1.375 GHz	= f_o
EXPECTED RESONANCE	$\simeq$ 1 GHz	
PARASITIC RESONANCE:	2.345 GHz	= f_p
USEABLE MODEL RANGE:	$\leq$1.006 GHz	= f_L

TABLE 2-3 OPTIMIZED PARAMETERS FOR DEVICE #2
(Line Width = 0.5 mil, Line Spacing = 0.2 mil, 5 turns)

OPTIMIZED INDUCTANCE:	4.6986 nhy $\pm$ 6.94%	= $L(\omega)$
EXPECTED INDUCTANCE:	12.11 nhy	
OPTIMIZED RESISTANCE:	14.973 ohms $\pm$ 5.75%	= $R(\omega)$
EXPECTED RESISTANCE:	9.6 ohms	
OPTIMIZED CAPACITANCE:	2.7826 pF $\pm$ 3.53%	= $C(\omega)$
ESTIMATED PARASITIC:	0.618 pF	= C/2
RESONANT FREQUENCY:	1.458 GHz	= f_o
EXPECTED RESONANCE:	$\approx$1 GHz	
PARASITIC RESONANCE:	2.954 GHz	= f_p
USEABLE MODEL RANGE:	$\leq$1.162 GHz	= g_L

TABLE 2-4 OPTIMIZED PARAMETERS FOR DEVICE #3

(Line Width = 0.8 mil, Line Spacing = 0.2 mil, 4 turns)

OPTIMIZED INDUCTANCE:	3.5076 nhy ± 7.86%	= $L(\omega)$
EXPECTED INDUCTANCE:	8.95 nhy	
OPTIMIZED RESISTANCE:	10.049 ohms ± 3.90%	= $R(\omega)$
EXPECTED RESISTANCE:	5 ohms	
OPTIMIZED CAPACITANCE:	3.9453 pF ± 4.16%	= $C(\omega)$
ESTIMATED PARASITIC:	1.521 pF	= C/2
RESONANT FREQUENCY:	1.368 GHz	= f_o
EXPECTED RESONANCE:	≈1 GHz	
PARASITIC RESONANCE:	2.179 GHz	= f_p
USEABLE MODEL RAGNE:	≤967 MHz	= f_L

3.0 TRANSISTOR MODELING[12]-[14]

A substantial percentage of GPS monolithic circuit design is accomplished by simulating and optimizing the response of proposed circuit topologies on the SPICE computer-aided circuit analysis program[15]. SPICE is capable of executing quiescent, small-signal linear, and large-signal transient behaviors of both active and passive networks. Its software includes routines for small-change sensitivity, Fourier, noise, and frequency response analyses of bipolar junction transistor, pn junction diode, JFET, and MOSFET circuits. Active device models are embedded within the program architecture. For junction transistors, the model utilized is a modified version of the Gummel-Poon structure which, unfortunately, requires some modification to render it amenable to the accurate simulation of circuits fabricated in the OAT (oxide aligned transistor) process. Even more significant is the fact that the determination of all required model parameters is a genuinely difficult task for which an established theory or computational methodology is unavailable.

Table 3-1 lists all of the MBJT parameters pertinent to a SPICE circuit simulation. Those which critically influence normal forward active device characteristics are encircled. The analytical details which follow focus almost exclusively on modeling as it relates to these 16 "forward" parameters, since the dynamical and quiescent effects of the remaining parameters listed in Table 3-1 are observable only for the case of a substantially forward biased base-collector junction. The enhanced analytical tractability afforded by the assumption that bipolar devices embedded in analog high frequency circuits are operated only in normal forward biasing regimes for all practical signal excursions is resultantly exploited, and default values are assigned to all of the non-encircled parameters appearing in Table 3-1. However, the default values suggested at the conclusion of this report are not necessarily those which have been recommended by the authors of SPICE.

TABLE 3-1 SPICE MBJT MODEL PARAMETERS

(Parameters which crucially affect the dynamics pertinent to forward active bias are encircled.)

Keyword	Parameter Name	Default Value	Units
(BF)	Ideal Forward Current-Gain Coefficient	100	----
BR	Ideal Reverse Current-Gain Coefficient	1	----
(IS)	Saturation Current	10^{-14}	amps
(RB)	Base Ohmic Resistance	0	ohms
(RC)	Collector Ohmic Resistance	0	ohms
(VA)	Forward Early Voltage	∞*	volts
VB	Reverse Early Voltage	∞*	volts
(IK)	Forward Knee Current	∞*	amps
(C2)	Forward Nonideal Base Current Coefficient	0	----
(NEL)	Nonideal B-E Emission Coefficient	2	----
IKR	Reverse Knee Current	∞*	amps
C4	Reverse Nonideal Base-Current Coefficient	0	----
NCL	Nonideal B-C Emission Coefficient	2	----
(Tf)	Forward Transit Time	0	sec
TR	Reverse Transit Time	0	sec
(CCS)	Collector-Substrate Capacitance	0	farads
(CJE)	Zero-Bias B-E Junction Capacitance	0	farads
(PE)	B-E Junction Potential	1	volts
(ME)	B-E Junction Grading Coefficient	0.5	----
(CJC)	Zero Bias B-C Junction Capacitance	0	farads

* Since VA, VB, IK, and IKR cannot be zero-valued, a zero value for these four parameters is interpreted to be an infinite value.

TABLE 3-1 SPICE MBJT MODEL PARAMETERS (concluded)

(Parameters which cruically affect the dynamics pertinent to forward active bias are encircled)

Keyword	Parameter Name	Default Value	Units
(PC)	B-C Junction Potential	1	volts
(MC)	B-C Junction Grading Coefficient	0.5	----
EG	Energy Gap	1.11	eV
PT	Saturation Current Temperature Exponent	3	----
KF	Flicker Noise Coefficient	0	----
AF	Flicker-Noise Exponent	2	----
Delay (TD)	Forward Transport Delay	0	sec or radians

It should be made clear at the outset that it is impossible to determine a unique model and corresponding parameter set leading to valid simulations of a broad variety of circuit responses. Thus, for example, a parameter set which delivers accurate steady-state results for low frequency small-signal excitations may not provide high integrity simulations of the response to high frequency small-signal inputs. Likewise, a satisfying parameter set for steady-state, low-frequency, small-signal analyses may be totally inappropriate for the investigation of the transient response to pulsed forcing functions.

This section of material overviews state-of-the-art MBJT model theory and documents a novel parameter determination technique which directly exploits the measured small-signal scattering (S) parameters of a given device. In contrast to traditional estimation procedures that focus directly on the problem of obtaining large-signal model parameters, the procedure developed as a part of this contract first extracts small-signal hybrid-pi parameters from S-parameter data, and then it utilizes these results in the computation of large-signal SPICE input data.

3.1 The MBJT Model

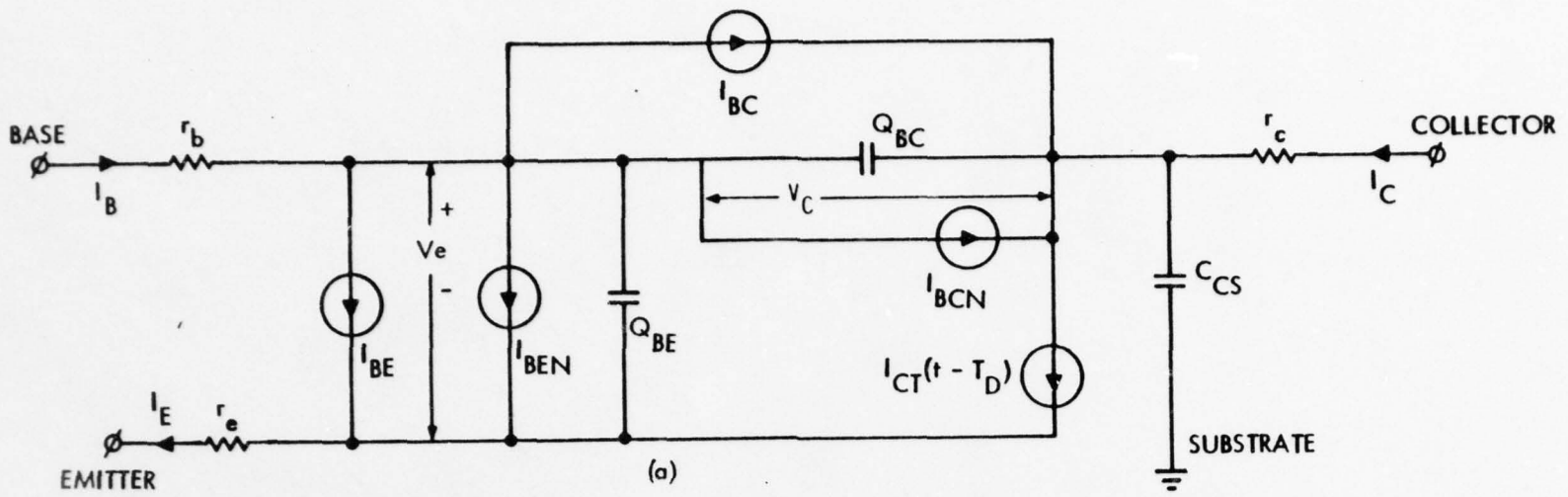
Figure 3-1a depicts the large-signal BJT model currently residing within SPICE program architecture. Current sources I_{BE} and I_{BEN} respectively represent the ideal and non-ideal components of base currents arising out of carrier injection from emitter-to-base, while I_{BC} and I_{BCN} have analogous significance for the base-collector junction. These four currents are defined by

$$I_{BE} = \frac{I_S}{B_F}(\varepsilon^{V_E/V_T} - 1) \tag{3-1}$$

$$I_{BEN} = C_2 I_S(\varepsilon^{V_E/N_{EL}V_T} - 1) \tag{3-2}$$

$$I_{BC} = \frac{I_S}{B_R}(\varepsilon^{V_C/V_T} - 1) \tag{3-3}$$

$$I_{BCN} = C_4 I_S(\varepsilon^{V_C/N_{CL}V_T} - 1). \tag{3-4}$$



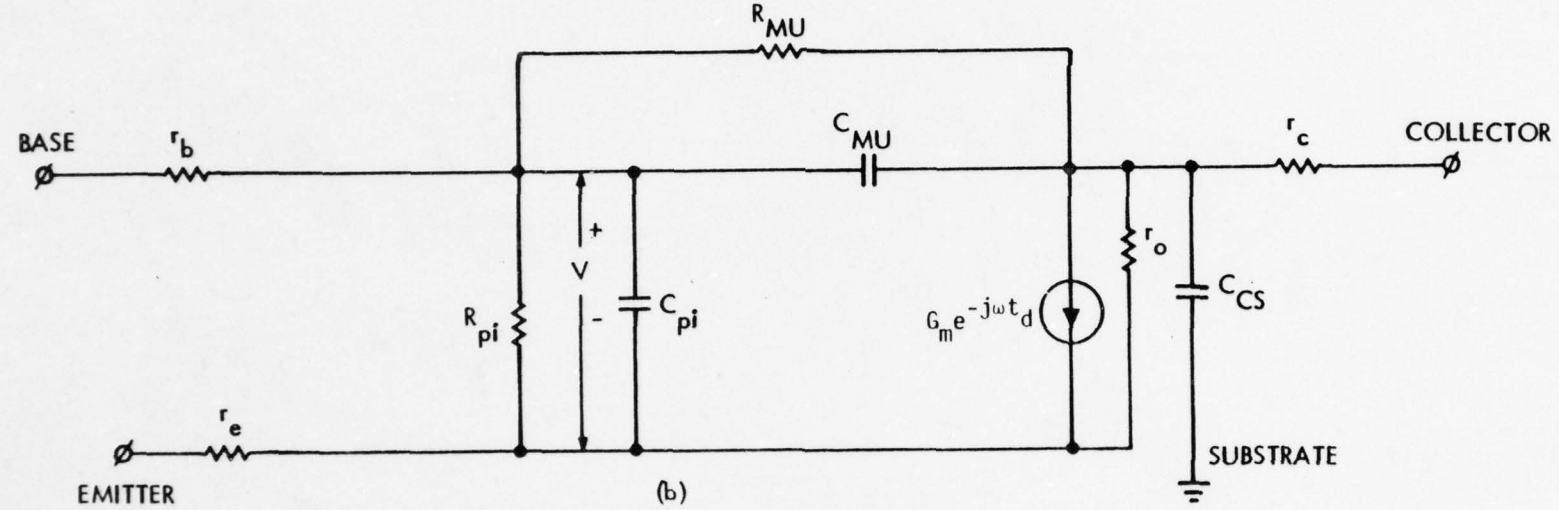


Figure 3-1 SPICE BJT Models (a) Large-Signal - (b) Small-Signal

By inspection of Table 3-1, it can be seen that B_F, I_S, C_2, N_{EL}, B_R, C_4, and N_{CL} in (3-1) through (3-4) are user-supplied input parameters. Moreover, V_E and V_C are the internal junction voltages defined in Figure 3-1a, while V_T is the familiar thermal voltage of the junction.

Current I_{CT} is the current transported to the collector as a direct ramification of charge injection across either junction. It is defined by

$$I_{CT} = \frac{I_S}{Q_{BN}}(\varepsilon^{V_E/V_T} - \varepsilon^{V_C/V_T}), \tag{3-5}$$

where Q_{BN} is the total charge, say Q_B, stored in the base region, normalized to the zero-bias or background charge concentration in the base. If Q_{BE} is the sum of charges due to injection from, and storage in, the vicinity of the emitter, and if Q_{BC} has analogous connotation for the collector region,

$$\frac{Q_B}{Q_{BO}} = Q_{BN} = \frac{Q_{BO} + Q_{BE} + Q_{BC}}{Q_{BO}} . \tag{3-6}$$

Charge parameter Q_{BN} relates to intrinsic junction voltages in accordance with,

$$Q_{BN} = \frac{Q_{1N}}{2} + \left\{\left(\frac{Q_{1N}}{2}\right)^2 + Q_{2N}\right\}^{1/2} \tag{3-7}$$

where

$$Q_{1N} = \left(1 - \frac{V_C}{V_A} - \frac{V_E}{V_B}\right)^{-1} \tag{3-8}$$

$$Q_{2N} = \left(\frac{I_S}{I_K}\right)(\varepsilon^{V_E/V_T} - 1) + \left(\frac{I_S}{I_{KR}}\right)(\varepsilon^{V_C/V_T} - 1). \tag{3-9}$$

Observe that V_A, V_B, I_K, and I_{KR} are fundamental input parameters. In SPICE, transport delay is simulated by appending a delay parameter, T_D to I_{CT}.

Resistance parameters, r_b, r_c, and r_e are user-defined quantities which model ohmic effects in base, collector, and emitter regions by constant linear resistances. Finally, C_{CS} is an input parameter which models substrate susceptance by a constant linear capacitance. The SUBSTRATE terminal is automatically connected to the node of greatest negative potential in the circuit being simulated.

When the small-signal or "AC" analysis routine is actuated, the SPICE program collapses the large-signal model of Figure 3-1a to the linearized structure shown in Figure 3-1b. In the linearized model,

$$\left.\begin{aligned} \frac{1}{R_{pi}} &= \frac{\partial I_B}{\partial V_E} \\ \frac{1}{R_{mu}} &= \frac{\partial I_C}{\partial V_C} \\ g_m &= \frac{\partial I_C}{\partial V_E} - \frac{\partial I_C}{\partial V_C} \\ \frac{1}{r_o} &= \frac{\partial I_C}{\partial V_{CE}} \end{aligned}\right\} \quad . \tag{3-8}$$

The small-signal effects of charge storage derive from

$$\left.\begin{aligned} C_{pi} &= \frac{\partial Q_{BE}}{\partial V_E} \\ C_{mu} &= \frac{\partial Q_{BC}}{\partial V_C} \end{aligned}\right\} \quad , \tag{3-9}$$

In (3-8) and (3-9) it is understood that all derivatives are evaluated at the quiescent operating point of the transistor, and

$$V_{CE} = -V_C + V_E \tag{3-10}$$

is the intrinsic collector-to-emitter voltage.

Experience gained by simulating the transient and small-signal steady-state responses of numerous analog circuits shows that the models depicted in Figure 3-1 suffer at least three shortcomings. First, high-frequency gain degradation caused by dynamic interaction of base

resistance and collector-base capacitance cannot be satisfactorily simulated by the presence of a single RC ($r_b C_{mu}$) section. Instead, a two section RC network proves more expedient for the simulation of high-frequency base region dynamics. Second, a single linear capacitance cannot adequately model charge storage dynamics of the collector-substrate interface. Rather, a series RC circuit, with C made voltage sensitive in accordance with the traditional depletion region approximation, is required. Finally, the topological placement of the substrate network turns out to be inappropriate for simulation of OAT dynamic characteristics. The substrate model should couple the substrate to the collector instead of to the intrinsic collector.

The problems enumerated above are eliminated by the proposed model revision portrayed in Figure 3-2a. Observe that the base resistance is partitioned into two components, r_{B1} and r_{B2}. This partitioning lends itself nicely to the implementation of a two-lump base comprised of r_{B1}, r_{B2}, C_{mu1}, and C_{mu2}, as shown in the counterpart small-signal model of Figure 3-2b. Problems in regard to substrate modeling are also alleviated by incorporation of the nonlinear voltage controlled current source, I_{CS}, which is defined by

$$I_{CS} = I_{SO}\left\{\epsilon^{V'_{CS}/V_T} - 1\right\} + \frac{dQ_{BS}}{dt} \tag{3-11}$$

where

$$V'_{CS} = V_{CS} - I_{CS}R_{CS} \tag{3-12}$$

and Q_{BS} is the charge stored in the collector-substrate interface.

3.2 Model Realization

The most satisfying way to implement the desired modeling revisions into SPICE is to re-program the pertinent SPICE subroutines. This is doubtlessly a worthwhile task, particularly if it is combined with other programming changes that are designed to enhance user rapport with computer-aided circuit analysis and design. Unfortunately, all required or desired changes to the SPICE code require more than trivial engineering effort. While cognate changes are tentatively planned for the near future, it is

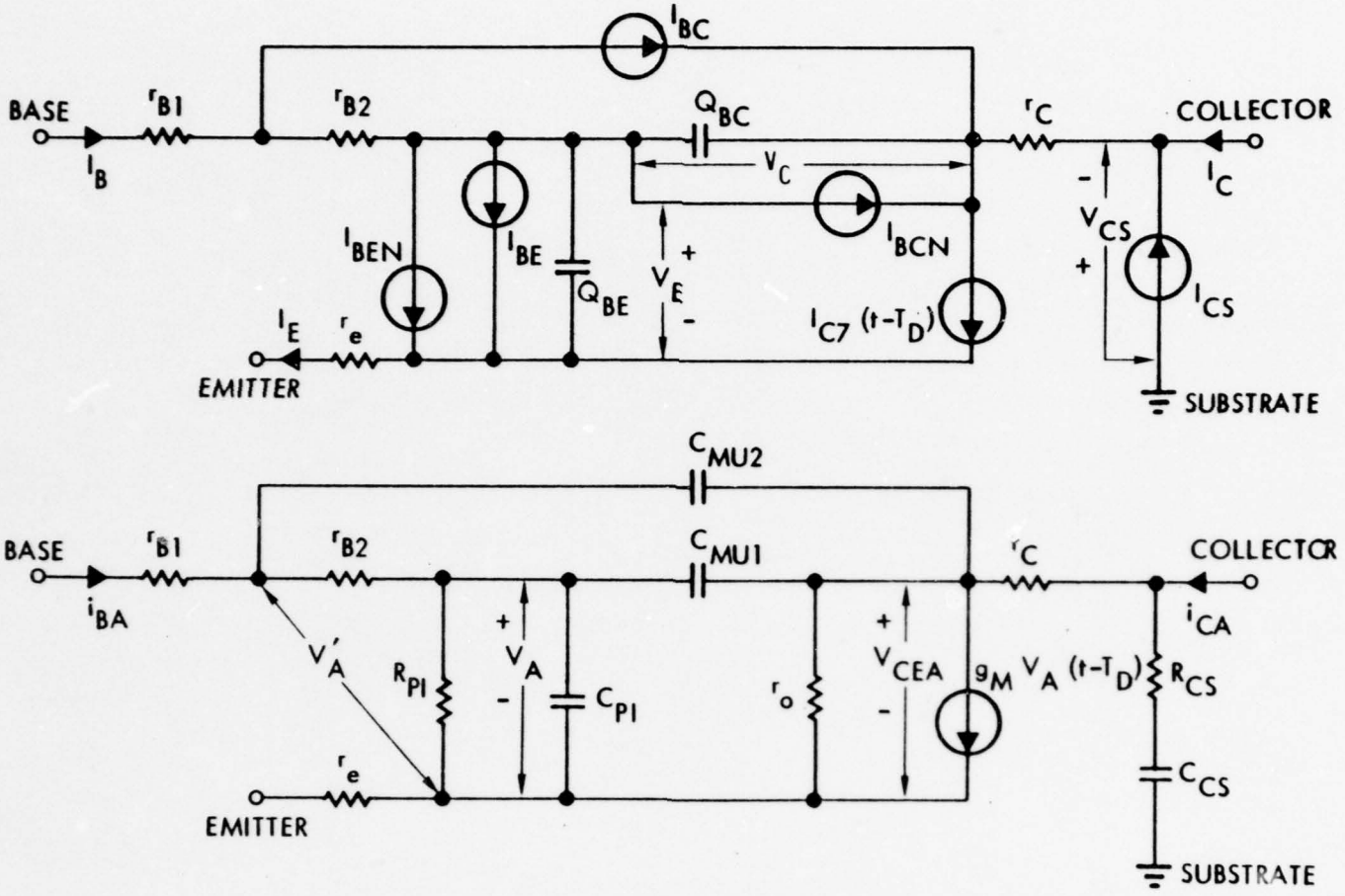


Figure 3-2 Proposed BJT Models (a) Large-Signal - (b) Small-Signal

fortunate that the revised model suggested in Figure 3-2a can be utilized immediately by using existing SPICE modeling capability to construct a macromodel or subcircuit for each OAT transistor of interest.

The OAT macromodel appears in Figure 3-3. Transistor Q is mathematically characterized by the parameters listed in Table 3-1, although care must be exercised to ensure the following keyword significances.

1. CCS, the collector-substrate capacitance is defaulted to zero. Substrate circuit dynamics are accounted for by diode DCS in the macromodel.

2. CJC, the zero-bias base-collector transition capacitance is set equal to the zero bias value of the transition component of C_{mu1} in Figure 3-2a. Diode DBC establishes the zero bias transition capacitance associated with C_{mu2}. For simplicity, the transition capacitance of C_{mu1} and C_{mu2} are assumed to possess identical junction potentials (PC) and junction grading coefficients (MC).

3. R_B, the base ohmic resistance of transistor Q is equated to r_{B2}. Resistance r_{B1} is an element in series with the external base terminal of the OAT device.

SPICE model parameters for semiconductor diodes are listed in Table 3-2. The following keyword significances must be understood.

1. R_S, the ohmic resistance, is defaulted to zero for diode DBC and is set equal to RCS for diode DCS.

2. Emission coefficient N, transit time TT, junction potential PB, and grading coefficient M for both diodes are respectively set equal to unity (1), TF, PC, and MC. The last three entities are transistor parameters pertinent to Q, as defined in Table 3-1.

3. CJO for diode DBC is equated to the zero-bias capacitance value associated with the transition component of C_{mu2}.

4. CJO for diode DCS is set equal to the zero bias substrate capacitance of the OAT device.

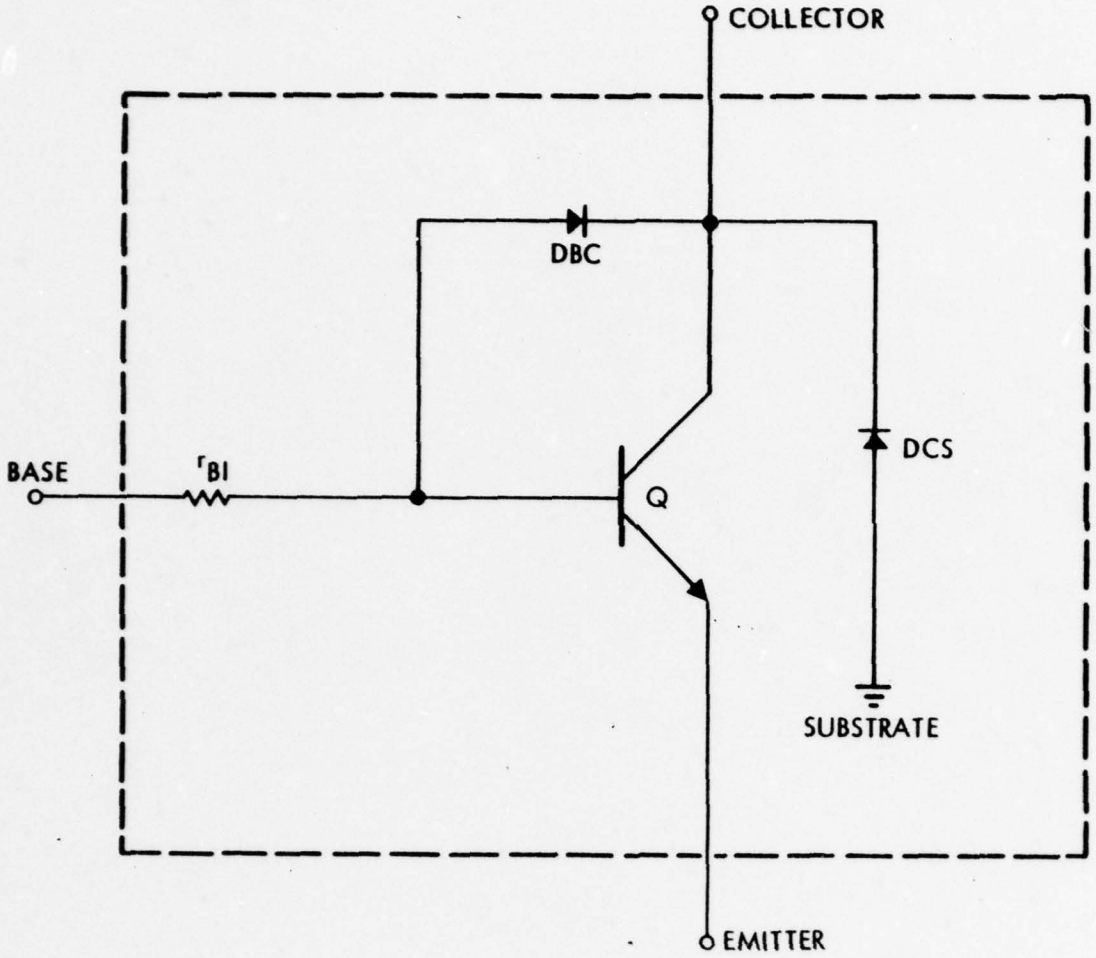


Figure 3-3 OAT Macromodel
Substrate terminal is electrically connected to most negative circuit nodes

TABLE 3-2 SPICE DIODE MODEL PARAMETERS

Keyword	Parameter Name	Default Value	Units
IS	Saturation Current	10^{-14}	amps
RS	Ohmic Resistance	0	ohms
N	Emission Coefficient	1	--
TT	Transit Time	0	sec
CJO	Zero-Bais Junction Capacitance	0	farads
PB	Junction Potential	1	volts
M	Grading Coefficient	0.5	----
EG	Energy Gap	1.11	eV
PT	Saturation Current Temp Exponent	3	----
KF	Flicker-Noise Coefficient	0	----
AF	Flicker-Noise Exponent	1	----

3.2.1 Parameter Optimization

The first step in the procedure to determine SPICE input parameters for the OAT process entails measurement of the magnitude and phase angle of each of the four (4) S-parameters at a number of frequencies and a given bias level for a given OAT device. The accuracy of parameter value estimations increases if attention is focused on a progressively more restricted frequency range over which S-parameters are monitored. Errors which invariably accrue if the frequency range is broadened can be somewhat offset if the number of frequencies sampled within a considered range is increased in proportion to the increase in measurement passband. In this study, the chosen range of frequencies extends from 800- MHz-to-2 GHz; the frequencies at which S-parameters were measured are 0.8, 1.0 , 1.2, 1.4, 1.6, 1.8, and 2.0 GHz. The 800 MHz-to-2 GHz range is appropriate for small-signal analyses through L-band and also, it is germane to the problem of ascertaining the large-signal transient responses to pulsed inputs having rise times that are no less than approximately 175pS.

The set of four S-parameters at each of the seven (7) sampled frequencies, along with the model topology of Figure 3-2b, are inputed into the COMPACT computer program[17]. COMPACT ascertains optimized values of each hybrid-pi model parameter. In particular, the COMPACT output is a numerical value for each of the 13 parameters which define the small-signal model of Figure 3-2b. This hybrid-pi parameter set ostensibly achieves the closest possible match between the measured S-parameters at each of the seven monitored frequencies and the respective S-parameters that might be predicted by the resultant hybrid-pi model at the same seven frequencies.

In order to confirm the adequacy of COMPACT results, the model of Figure 3-2b is exercised in the SPICE program to obtain hybrid (or h-) parameter two-port data at each of the test frequencies. SPICE results are compared with experimental observations by converting S-parameter data to equivalent h-parameter data. Additionally, quiescent gain and transfer characteristics are measured and corroborated with SPICE simulations. Preliminary results on numerous test devices indicate

that the absolute percentage error between measured and analytical magnitudes of any h-parameter at any of the seven test frequencies and at zero frequency is less than 9%. Corresponding phase errors are less than 10 degrees in magnitude.

The final step in the parameter determination methodology is to determine the corresponding large-signal input parameters which uniquely define the optimized small-signal model elements produced by COMPACT. This problem is addressed in the subsequent subsection. A flow chart which overviews the foregoing methodology is offered in Figure 3-4.

3.2.2 Large-Signal Parameters

The net base current, I_B, flowing in the model of Figure 3-2a is

$$I_B = I_{BEN} + I_{BE} + I_{BC} + I_{BCN} + \frac{d(Q_{BE} + Q_{BC})}{dt}, \tag{3-13}$$

where Q_B is given by (3-6) and it is recalled that Q_{BO} in (3-6) is a constant charge parameter. Equation (3-13) is easily linearized by expanding it into a Taylor series expansion about the quiescent base current and retaining only those terms in the expansion which are linearly dependent upon intrinsic junction voltages and their first derivatives. When this analytical procedure is pursued, the small-signal component of total base current is found to be of the form,

$$i_{BA} = (\frac{1}{R_{pi}})V_A + C_{pi}(\frac{dV_A}{dt}) + C_{mu}\frac{d}{dt}(V_A - V_{CEA}). \tag{3-14}$$

In arriving at (3-14), the conductances associated with I_{BC} and I_{BCN} are ignored in deference to the presumption that the collector-base junction is reverse biased; i.e., $V_C < 0$. From (3-3) and (3-4), the resultant small-signal dynamic conductances are seen to approach zero for $V_C < 0$. Moreover, using (3-1) and (3-2)

$$\frac{1}{R_{pi}} = \frac{\partial(I_{BEN} + I_{BE})}{\partial V_E} = \frac{1}{N_{EL}V_T}\left\{I_{BQ} + (N_{EL} - 1)I_{BEO}\right\}, \tag{3-15}$$

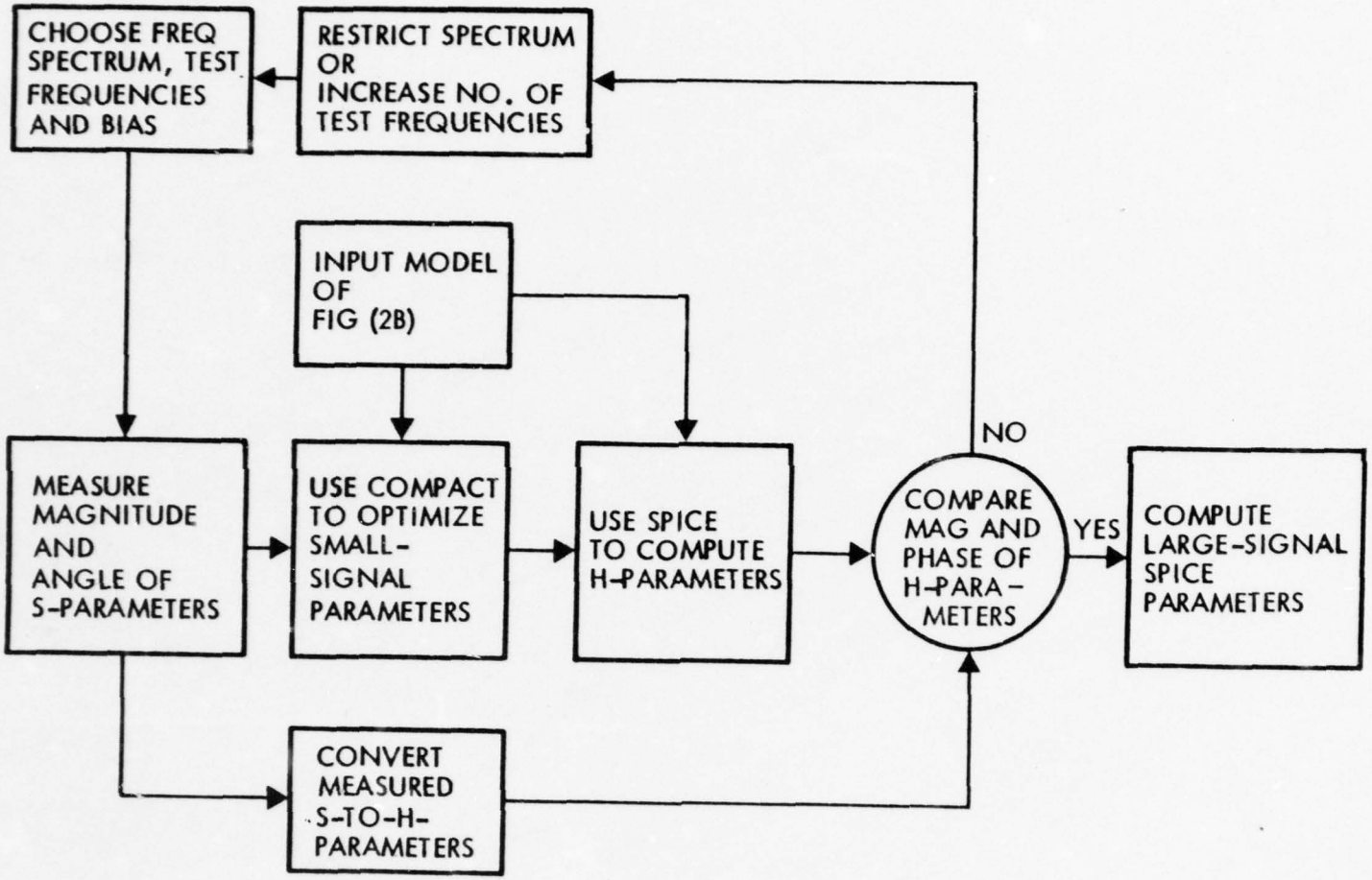


Figure 3-4 Flowchart of Parameter Determination Technique

where subscript Q connotes quiescent or static quantities. Finally,

$$C_{pi} = \frac{\partial(Q_{BE} + Q_{BC})}{\partial V_E} \tag{3-16}$$

$$C_{mu} = \frac{\partial(Q_{BE} + Q_{BC})}{\partial V_C} \quad , \tag{3-17}$$

where V_C is recognized as being $(V_E - V_{CE})$ and $V_A(V_{CEA})$ represents the small-signal component of the instantaneous value of voltage $V_E(V_{CE})$.

Ignoring substrate conductance, the effects of which can be appended later without loss of accuracy or generality, the net instantaneous collector current in Figure 3-2a is

$$I_C = I_{CT} - (I_{BC} + I_{BCN}) - \frac{dQ_{BC}}{dt} \quad . \tag{3-18}$$

A procedure analogous to that invoked in reducing (3-13) to (3-14) produces for the small-signal collector current

$$i_{CA} = g_m V_A(t - T_D) + \frac{1}{r_o} V_{CEA} + C_{mu} \frac{d}{dt}(V_{CEA} - V_A). \tag{3-19}$$

In (3-19)

$$g_m \triangleq g_{mf} - 1/r_o \tag{3-20}$$

and

$$g_{mf} = \frac{\partial I_{CT}}{\partial V_E} \simeq \frac{I_{CQ}}{V_T}(1 - V_T S_{QE}), \tag{3-21}$$

$$\frac{1}{r_o} = - \frac{\partial I_{CT}}{\partial V_C} \simeq I_{CQ} S_{QC}. \tag{3-22}$$

In (3-21) and (3-22) S_{QE} and S_{QC} are the normalized charge sensitivity functions,

$$S_{QE} \triangleq \frac{\partial Q_{BN}/Q_{BN}}{\partial V_E} \quad , \tag{3-23}$$

$$S_{QC} \triangleq \frac{\partial Q_{BN}/Q_{BN}}{\partial V_C} \quad . \tag{3-24}$$

If the transistor does not enter high injection regimes, $Q_{BN} \simeq Q_{1N}$,

$$S_{QE} \simeq \frac{1}{V_B\left(1 - \frac{V_C}{V_A} - \frac{V_E}{V_B}\right)} = \frac{Q_{1N}}{V_B} \tag{3-25}$$

$$S_{QC} \simeq \frac{1}{V_A\left(1 - \frac{V_C}{V_A} - \frac{V_E}{V_B}\right)} = \frac{Q_{1N}}{V_A} \tag{3-26}$$

The foregoing two expressions can be further simplified to $1/V_B$ and $1/V_A$, respectively, if the forward and reverse Early voltages are large in comparison with the magnitude of junction voltage biases.

The capacitance expressions are evaluated through use of (3-6) and (3-7).

$$C_{pi} = \frac{\partial Q_{EO}}{\partial V_E} + \frac{\partial Q_E}{\partial V_E} + \frac{\partial Q_{CO}}{\partial V_E} + \frac{\partial Q_C}{\partial V_E} \quad . \tag{3-27}$$

The first term in this equation evaluates to the form,

$$\frac{Q_{EO}}{V_E} = C_{JE}\left[1 - \frac{V_E}{P_e}\right]^{-M_e} \tag{3-28}$$

Since $V_C < 0$ is tacitly presumed,

$$Q_E \simeq \frac{Q_{BO}}{I_K} I_{CT} \quad , \tag{3-29}$$

whence

$$\frac{\partial Q_E}{\partial V_E} = T_{FE} g_{mF}, \tag{3-30}$$

where

$$T_{FE} \triangleq \frac{Q_{BO}}{I_K} \tag{3-31}$$

is noted as the effective forward transit time of the device. In the SPICE BJT model, T_{FE} is made proportional to the net base charge, Q_B, by writing

$$T_{FE} \triangleq T_F Q_{BN} \tag{3-32}$$

where T_F is a fundamental program input parameter. Equation (3-32) comprises a crude first order mathematical definition of base pushout which is tantamount to an effective widening of the base when excessive charge storage materializes in the base region. This base widening or "pushout" model is the mathematical artifax usually invoked to explain gain-bandwidth product degradation at high collector currents and low collector-emitter voltages.

Returning to (3-27), the third term on the right hand side is zero by virtue of the fact that Q_{CO} is independent of V_E. Moreover, the last term can be ignored in deference to the reverse-biased collector assumption. It follows that

$$C_{pi} = \frac{C_{JE}}{\left(1 - \frac{V_E}{P_e}\right)^{M_e}} + T_F Q_{BN} g_{mF}. \tag{2-33}$$

In similar fashion, it can be shown that (3-17) evaluates as

$$C_{mu} = T_F \left(\frac{I_S}{V_T}\right)\left(\frac{I_K}{I_{KR}}\right)\left(\varepsilon^{V_C/V_T}\right) + \frac{C_{JC}}{\left(1 - \frac{V_C}{P_C}\right)^{M_e}}. \tag{3-34}$$

In arriving at this result (3-31) and (3-32) are utilized, and the relative insensitivity of Q_E to V_C for $V_C < 0$ is exploited. Actually, the SPICE code computes the first term on the right hand side of (3-34) as

$$\frac{T_R I_S}{V_T}\left(\varepsilon^{V_C/V_T}\right),$$

where T_R is a fundamental input parameter. This computational procedure is equivalent to irradication of input parameter I_{KR}, which is used only in dc or static analyses, and thence, computation of an "ac" value of I_{KR} say I_{KR}', such that

$$T_R = T_F \frac{I_K}{I_{KR}'} .$$

The procedure in question is inconsistent and arises only because of the base pushout model inferred by (3-32). This inconsistency generates potentially serious errors since the resultant expression for C_{mu} is divorced of a strong diffusion component which materializes when base pushout necessarily mandates a forward biased intrinsic collector junction.

Two additional steps remain in order to render plausible the small-signal model of Figure 3-2a. First, the mathematical existence of the two-lump base approximation can be argued by postulating in (3-18) that

$$C_{mu} \frac{d}{dt}(V_{CEA} - V_A) = C_{mu1} \frac{d}{dt}(V_{CEA} - V_A) + C_{mu2} \frac{d}{dt}(V_{CEA} - V_A'). \quad (3\text{-}35)$$

To the extent that the intrinsic collector-base junction is indeed reverse biased, both C_{mu1} and C_{mu2} can be presumed to possess identical junction potentials and identical grading coefficients. Second, the substrate branch in Figure 3-2b can now be appended by setting

$$C_{CS} = \frac{C_{JO}}{\left(1 - \frac{V_{CS}'}{P_B}\right)^M} . \quad (3\text{-}36)$$

The form of this capacitance expression, along with tacit neglect of any dynamic conductance which might be evidenced across the intrinsic junction of the substrate diode, presumes that the collector-substrate port is reverse biased.

3.3 Parameter Determination

As explained earlier, the independent variables which are available for SPICE-2 parameter identification are the 13 small-signal parameters which comprise the topological definition of the model in Figure 3-2b. These 13 parameters, which are optimized for an appropriate frequency passband at various bias settings, are the "known" variables which serve as inputs to the final computational block in Figure 3-4.

3.3.1 Substrate Branch

Resistance R_{CS} is modeled as a simple constant. It is not likely that R_{CS} varies appreciably over a monitored range of substrate voltage. Accordingly, it seems appropriate to set R_S for diode DCS in Figure 3-3 equal to the average of R_{CS} determinations; i.e.,

$$R_S(DCS) = \bar{R}_{CS} \tag{3-37}$$

whee the bar symbolizes averaging with respect to values enumerated by COMPACT at various substrate voltages.

Assuming all measurements are conducted for a non-forward-biased substrate, (3-12) gives $V'_{CS} \simeq V_{CS}$. Since the substrate branch is made to appear across the collector-to-ground port, $V_{CS} = -V_{CE}$, the quiescent collector voltage with emitter grounded. Then by (3-36),

$$C_{JO} \simeq C_{CS}\left(1 + \frac{V_{CE}}{P_B}\right)^M . \tag{3-38}$$

Clearly, C_{JO} is the value measured as C_{CS} for very small V_{CE}; i.e.,

$$C_{JO}(DCS) = C_{CS}\Big|_{V_{CE} \simeq 0.} \tag{3-39}$$

Because the collector region possesses a graded impurity profile,

$$M \simeq 0.333. \tag{3-40}$$

It follows that if $C_{CS} = C_{CX}$ at $V_{CE} = V_{CEX} > 0$,

$$P_B = \frac{V_{CEX}}{\left(\frac{C_{JO}}{C_{CX}}\right)^3 - 1} . \tag{3-41}$$

Summary-Substrate

A). Obtain R_{CS} and C_{CS} at a minimum of two V_{CE} values, say $V_{CE} \simeq 0$ and $V_{CE} \simeq V_{CEX} > 0$.

B). Use (3-37) to determine R_S for diode DCS.

C). Use (3-39) to determine C_{JO} for diode DCS.

D). Default M in accordance with (3-40)

E). Use (3-41) to determine P_B for diode DCS.

3.3.2 Diode DBC and Capacitor C_{mul}

The expression for C_{mu2} is

$$C_{mu2} \simeq \frac{C_{JO}(DBC)}{\left(1 + \frac{V_{CB}}{P_C}\right)^{M_C}} , \tag{3-42}$$

where M_c is set equal to 0.333. By analogy to previous considerations,

$$C_{JO}(DBC) = C_{mu2}\Big|_{V_{CB} \simeq 0.} \tag{3-43}$$

and

$$P_c = \frac{V_{CBX}}{\left[\frac{C_{JO}(DBC)}{C_{mu2X}}\right]^3 - 1} . \tag{3-44}$$

Similarly,

$$C_{mul} \simeq \frac{C_{JC}}{\left(1 + \frac{V_{CB}}{P_c}\right)^{M_c}} \quad , \tag{3-45}$$

whence

$$C_{JC} = C_{mul}\Big|_{V_{CB} = 0} \cdot \tag{3-46}$$

Summary - DBC and C_{mul}

A). Equate C_{JO} for diode DBC to the value of C_{mu2} determined for very small-collector-base voltage. For this same small voltage, equate C_{JC} in Table 3-1 to C_{mul}.

B). Set M for diode DBC equal to M_c and choose $M_c \simeq 1/3$.

C). Set P_B for diode DBC equal to P_c and calculate P_c from (3-44), with V_{CBX} representing the positive collector-base voltage at which the measured value of C_{mu2} is C_{mu2X}.

3.3.3 Ohmic Resistances

Resistances r_{B1}, r_{B2}, r_e, and r_c are determined directly by COMPACT. No further computations related to these parameters are required.

3.3.4 Early Voltages

From (3-20) through (3-22),

$$g_{mF} = \frac{1}{r_o} + g_m = \frac{1 + g_m r_o}{r_o} \quad , \tag{3-47}$$

$$S_{QE} = \frac{I_{CQ} - g_{mF} V_T}{I_{CQ} V_T} \tag{3-48}$$

$$S_{QC} = \frac{1}{r_o I_{CQ}} . \tag{3-49}$$

The left hand sides of these three equations are easily evaluated if the collector bias current corresponding to COMPACT enumerations of g_m and r_o are recorded. Then from (3-25) and (3-26),

$$V_A = \frac{1 + S_{QE}V_{CE} - (S_{QE} + S_{QC})V_{CB}}{S_{QC}} \tag{3-50}$$

$$V_B = \frac{S_{QC}}{S_{QE}}V_A = \frac{1 + S_{QE}V_{CE} - (S_{QE} + S_{QC})V_{CB}}{S_{QE}} . \tag{3-51}$$

In (3-50) and (3-51), V_C is replaced by $(-V_{CB})$ and use is made of the fact that

$$V_{CE} = V_{CB} + V_E. \tag{3-52}$$

Summary - V_A and V_B

A). For given bias (V_{CE}, V_{CB}, and $I_C = I_{CQ}$), compute g_{mF}, S_{QE}, and S_{QC} from (3-47) through (3-49).

B). Compute V_A and V_B from (3-50) and (3-51).

3.3.5 T_F, I_S, I_K

Parameters T_F and I_K can be determined by exploiting capacitance C_{pi} in Figure 3-2b at two collector voltages. Consider first the case of moderate current and moderate collector voltage. Under such an operating condition, the second term on the right hand side of (3-33) far outweighs the transition component of C_{pi} so that

$$C_{pi} \approx T_F Q_{BN} g_{mF}. \tag{3-53}$$

But $Q_{BN} \approx Q_{1N}$ if the collector current is not too large and by virtue of (3-22) and (3-26),

$$C_{pi} = \frac{T_F g_{mF} V_A}{I_{CQ} r_o} ,$$

Accordingly,

$$T_F \simeq \left(\frac{I_{CQ}}{g_{mF}}\right)\left(\frac{r_o}{V_A}\right) C_{pi} , \tag{3-54}$$

where it is understood that both g_{mF} and C_{pi} are determined at the same bias condition.

Now, reconsider (3-33) at the same collector current (I_{CQ}) for which T_F has been determined, but at a significantly smaller collector voltage. If C_{pi2} and g_{mF2} respectively signify C_{pi} and g_{mF} at this second bias condition

$$Q_{BN2} \simeq \frac{C_{pi2}}{T_F g_{mF2}} . \tag{3-55}$$

For given junction voltages, Q_{1N2} can be computed from (3-8) whence, by (3-7)

$$Q_{2N2} = Q_{BN2}(Q_{BN2} - Q_{1N2}). \tag{3-56}$$

Equation (3-9) can now be used to determine

$$\frac{I_S}{I_K} \simeq Q_{2N2} \varepsilon^{-V_{E2}/V_T} , \tag{3-57}$$

where $V_{E2} = V_{CE} - V_{CB}$ is the base-emitter voltage appropriate to the bias at which (3-55) is determined.

Equation (3-5) now provides the vehicle by which I_S and I_K can be individually determined. In particular,

$$I_S = Q_{BN2} I_{CQ} \varepsilon^{-V_{E2}/V_T} ; \tag{3-58}$$

when combined with (3-56) and (3-57), this result yields

$$I_K = \frac{I_{CQ}}{Q_{BN2} - Q_{1N2}} . \tag{3-59}$$

Summary - T_F, I_S, I_K

A). Determine hybrid-pi model parameters at two collector voltages, V_{CE2} and V_{CE1} ($V_{CE1} >> V_{CE2}$) and for each collector voltage, ensure that the collector current, I_{CQ}, is identical and moderate in value (greater than about 2 mA).

B). Find T_F from (3-54) at $I_C = I_{CQ}$ and $V_{CE} = V_{CE1}$.

C). At $I_C = I_{CQ}$ and $V_{CE} = V_{CE1}$, determine Q_{BN2} and Q_{1N2} from (3-55) and (3-8).

D). Find I_S and I_K from (3-58) and (3-59).

3.3.6 C_{pi} Transition Component

There is no accurate way of determining C_{JE}, P_e, and M_e in (3-33) unless the transistor in question is characterized under reverse bias conditions or unless accurate plots of f_T (common emitter gain-bandwidth product) are generated, particularly at low collector currents. If reverse bias characterizations are obtained, the procedure itemized in Section 3.3.2 is applicable, with the proviso that $M_e \approx 0.5$. Then, since the second term in (3-33) is negligible for a back-biased base-emitter junction,

$$C_{JE} = C_{pi}\big|_{V_E = 0} \tag{3-60}$$

$$P_e = \frac{V_{EX}}{\left[\dfrac{C_{JE}}{C_{pi}\big|_{V_{EX}}}\right]^2 - 1} . \tag{3-61}$$

3.3.7 f_T Prediction

The use of common-emitter gain-bandwidth product to predict C_{JE}, P_e, and other program input parameters deserves at least cursory attention in this report. To the extent that r_e and r_c in Figure 3-2a can be ignored, the SPICE-2 program evaluates f_T in accordance with

$$2\pi f_T \simeq \frac{g_m}{C_{pi} + C_{mul} + \frac{r_{B2}}{R_{pi}} C_{mu2}} . \tag{3-62}$$

At small current levels, the term involving R_{pi} can be ignored, as can the second term on the right hand side of (3-33). Thus, (3-62) becomes

$$2\pi f_T \Big| I_{CQ} \to 0 \simeq \frac{g_m}{C_{JE}(V_E) + C_{mul}} , \tag{3-63}$$

where $C_{JE}(V_E)$ symbolizes the first term on the right hand side of (3-33). By (3-20), (3-21), and (3-25)

$$2\pi f_T \Big| I_{CQ} \to 0 \simeq \frac{I_{CQ}(1 - V_T Q_{1N}/V_B)}{V_T[C_{JE}(V_E) + C_{mul}]} , \tag{3-64}$$

where it is tacitly assumed that $g_{mF} >> 1/r_o$. If the collector-base bias voltage is held fast, the fact that base-emitter bias is virtually constant for restricted intervals of small-collector current can be exploited to assert that the slope say M_F, in the f_T versus I_{CQ} characteristic is constant at the value of

$$M_F \simeq \frac{1 - V_T Q_{1N}/V_B}{2\, V_T[C_{JE}(V_E) + C_{mul}]} . \tag{3-65}$$

The measured low current slope can be combined with the results of the preceding six parameter determination steps to ascertain $C_{JE}(V_E)$. Actually, M_F can be measured at two low collector currents, corresponding to two values of V_E, to determine C_{JE} and P_e, with M_e set equal to 1/2.

At progressively larger currents, (3-62) converges toward g_m/C_{pi} and using (3-33)

$$2\pi f_T \simeq \frac{1}{T_F Q_{BN}} , \tag{3-66}$$

where the first term on the right hand side of (3-33) is ignored and once again, it is assumed that $g_m \simeq g_{mF}$. At moderate currents, $Q_{BN} \simeq Q_{1N}$ and, recalling (3-8), (3-66) shows that for constant V_C, f_T approaches a constant asymptote. As forward bias at the base-emitter junction is made to increase, Q_{BN} increases in accordance with (3-7) through (3-9), and f_T resultantly degrades. The rate of f_T degradation with current is identical to the h_{FE} degradation rate. The situation described is shown in Figure 3-5.

3.3.8 Delay

Parameter T_D is obtained directly from the measured scattering parameter, $S_{21}(j\omega)$. This parameter nominally obeys the relationship,

$$S_{21}(j\omega) = \left\{\frac{S_{21}(0)}{1 + j\omega/\omega_s}\right\} \varepsilon^{-j\omega T_D} . \tag{3-67}$$

At two radial frequencies, say ω_1 and ω_2, one may glean ω_s by comparing magnitudes of $S_{21}(j\omega)$. In particular,

$$\left|\frac{S_{21}(j\omega_2)}{S_{21}(j\omega_1)}\right| = \left\{\frac{1 + (\omega_2/\omega_s)^2}{1 + (\omega_1/\omega_s)^2}\right\}^{1/2} \tag{3-68}$$

Once ω_s is known, the measured phase, say $\phi_{21}(\omega)$, at any frequency may be used to discern T_D, since

$$\phi_{21}(\omega) = -\omega T_D - \text{TAN}^{-1}\left(\frac{\omega}{\omega_s}\right) . \tag{3-69}$$

Summary - T_D

A). Measure magnitudes of $S_{21}(j\omega)$ at two frequencies, ω_1 and ω_2.

B). Use (3-68) to determine ω_s.

C). For a measured phase angle of $S_{21}(j\omega)$ and the computed ω_s, (3-69) can be used to find T_D.

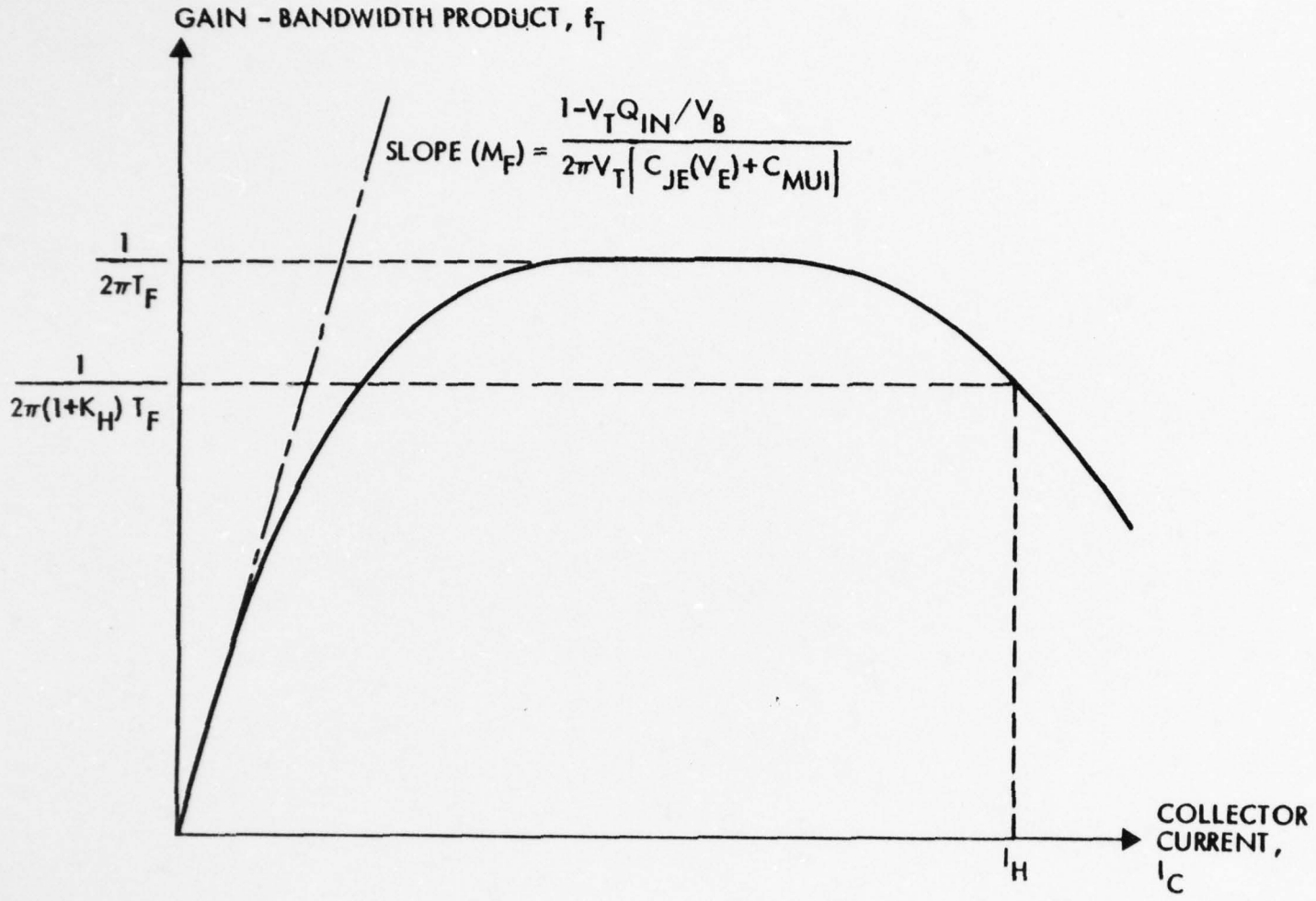


Figure 3-5 Typical SPICE-2 Prediction of Common Emitter Gain Bandwidth Product as a Function of Collector Current

3.3.9 B_F, C_2, N_{EL}

At moderate current levels, $I_{BQ} \simeq I_{BEQ}$ in (3-15) so that

$$\frac{1}{R_{pi}} \simeq \frac{I_{BQ}}{V_T} . \tag{3-70}$$

Moreover, (3-21) and (3-25) produce

$$g_{mF} \simeq g_m = \frac{I_{CQ}}{V_T}(1 - V_T Q_{1N}/V_B). \tag{3-71}$$

It follows that

$$g_m R_{pi} = h_{FE}(1 - V_T Q_{1N}/V_B), \tag{3-72}$$

because

$$h_{FE} \triangleq \frac{I_{CQ}}{I_{BQ}} \tag{3-73}$$

is the large-signal transistor "beta." Since V_B, g_m, and R_{pi} are known at the bias level of interest, and since Q_{1N} is easily computed for this bias level, h_{FE} is straight-forwardly computed as

$$h_{FE} = \frac{g_m R_{pi}}{1 - V_T Q_{1N}/V_B} . \tag{3-74}$$

If the bias level chosen is appropriate for neglect of Q_{2N},

$$B_F = \left(\frac{Q_{1N}}{\frac{V_T}{1 - (\frac{V_T}{V_B})Q_{1N}}} \right) g_m R_{pi} . \tag{3-75}$$

Note, however, that Q_{2N} need not be ignored, since at this juncture, I_S and I_K, which determine Q_{2N}, are known quantities.

The only reasonably accurate technique for the estimation of C_2 and N_{EL} is to measure h_{FE} as a function of collector current. In particular, at least two values of I_L must be measured, and the log-log plot of I_C/I_S versus inverse degradation factor, $1/K_L$, expedites the parameter determination process. This statement derives from

$$\text{Log}\left(\frac{I_L}{I_S}\right) = \left(\frac{N_{EL}}{N_{EL} - 1}\right)\left[\text{Log}C_2 + \text{Log}\left(\frac{1}{K_L}\right)\right] \quad , \tag{3-76}$$

which infers a slope of $N_{EL}/(N_{EL} - 1)$. Moreover, with $K_L = 1$ (factor of 2 degradation in h_{FE}), C_2 is easily evaluated. Figure 3-6 displays these assertions.

Summary - B_F, C_2, N_{EL}

A). For a moderate current bias level, calculate B_F from (3-75).

B). Measure h_{FE} at very low collector currents and determine current I_L at which h_{FE} degrades by $(1 + K_L)$ for at least two values of $I_C = I_L$. Plot results in the form of Figure 3-6.

C). Determine N_{EL} from slope of aforementioned plot. Determine C_2 by reading $\text{Log}(I_L/I_S)$ at any other value of K_L (e.g., $K_L = 1$).

3.3.10 Default Parameters

Parameter T_R can be set equal to 1000 T_F, to reflect the fact that a transistor operated in inverse mode is at least two-to-three orders of a magnitude slower than one biased for normal active operation.

Recalling (3-34), default parameter I_{KR} to

$$I_{KR} = \left(\frac{T_F}{T_R}\right)I_K \simeq I_K/1000. \tag{3-77}$$

The suggested default values for E_G, P_T, K_F, and A_F in Table 3-1 can be utilized directly. The same statement also applies for C_4 and N_{CL} in this table.

Finally, experience has shown that high-frequency integrated circuit transistors generally exude a reverse current gain coefficient, β_R, that is less than unity. Accordingly, set β_R to approximately 0.8.

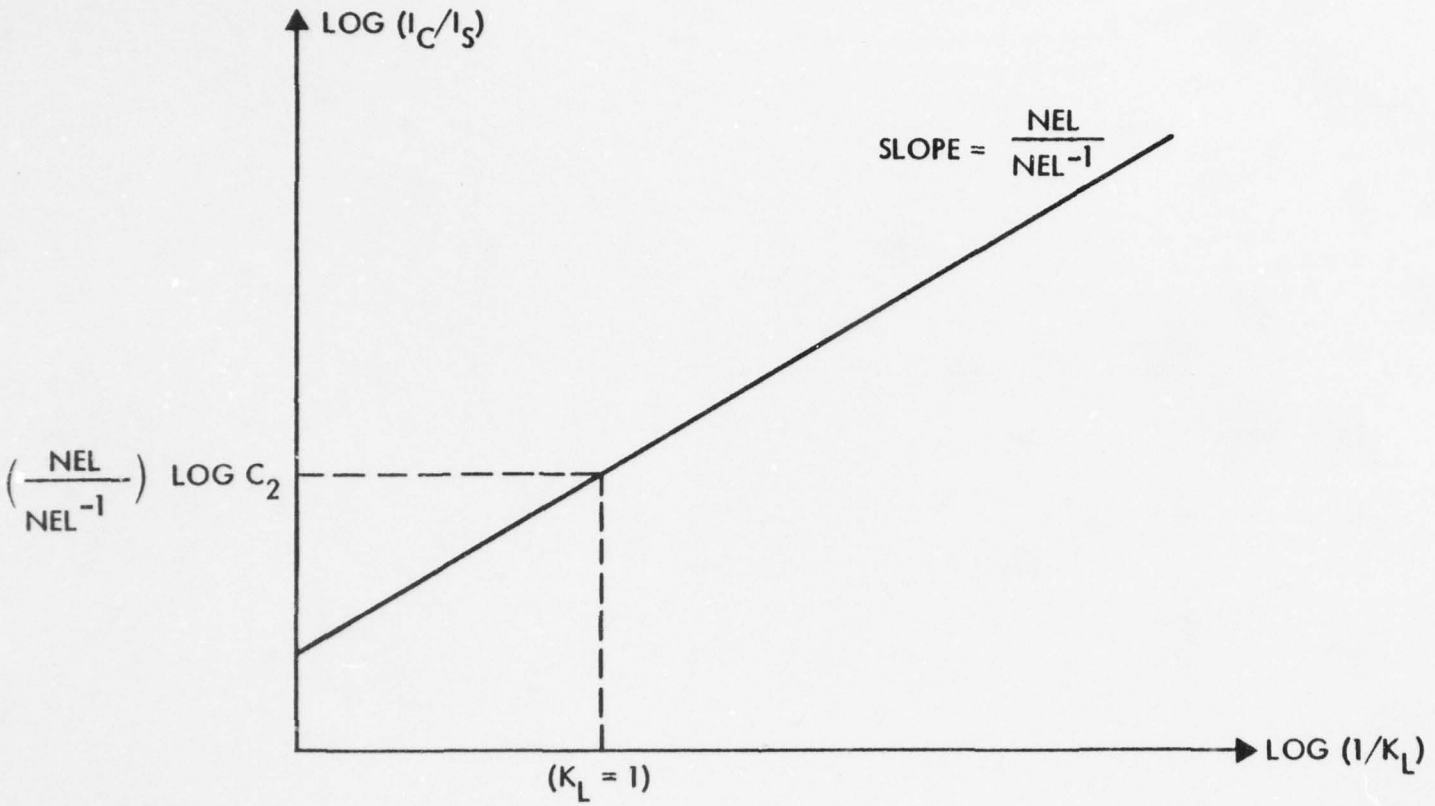


Figure 3-6 Low Current Degradation Characteristics of h_{FE}. Current I_L is the collector current at which h_{FE} degrades by $(1 + K_L)$.

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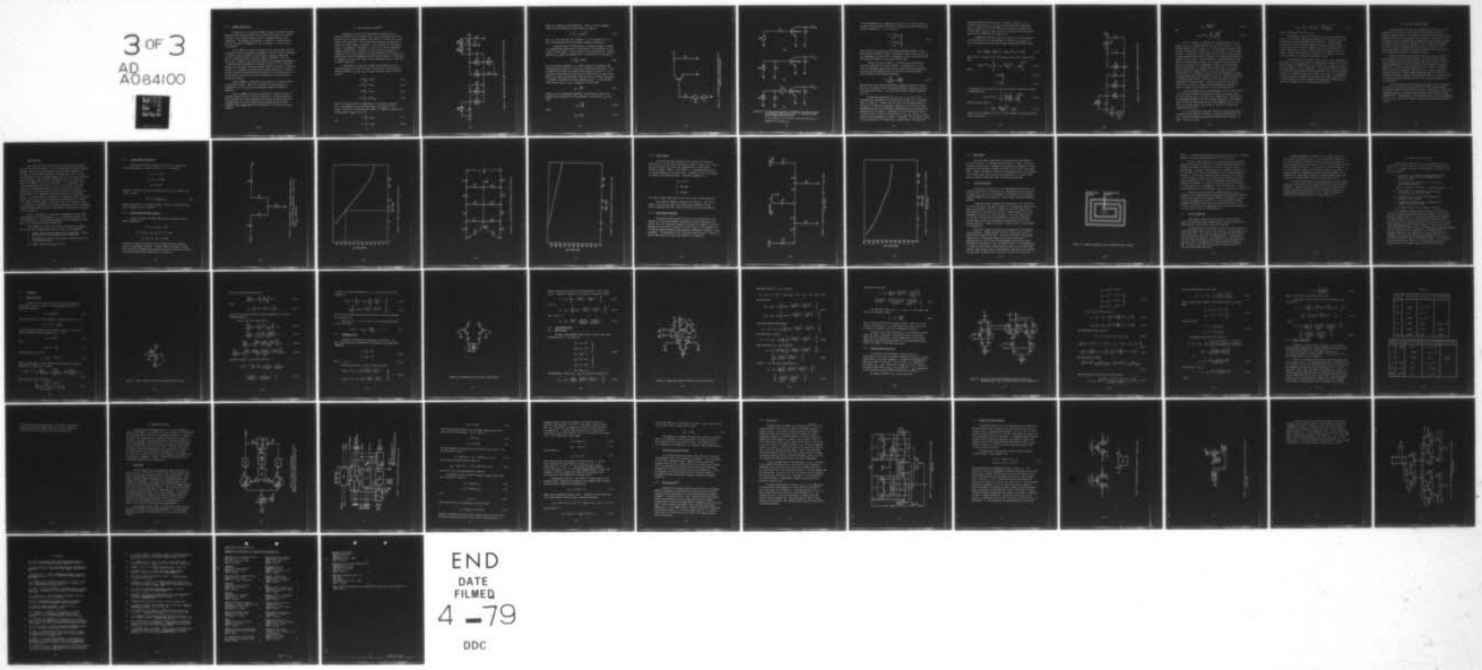

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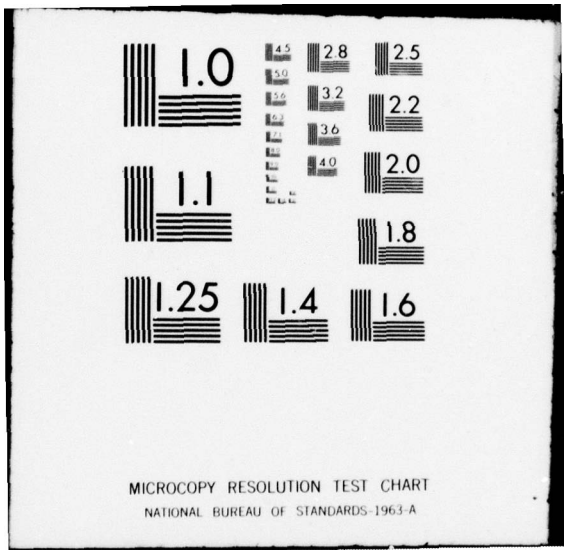
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3.4 COMPACT Simulations

In addition to utilizing the COMPACT program in the MBJT parameter determination procedure, COMPACT has also been used directly to simulate the small-signal response characteristics of proposed amplifier configurations. The numerous disadvantages to COMPACT, as itemized below, has led to a general de-emphasis of its utilization in circuit simulation ventures.

First, COMPACT is capable of executing only small-signal analyses. It operates directly on measured S-parameters, converts inputed S-parameters to two-port hybrid parameters, and proceeds to execute a linearized analysis predicated solely on two-port network theory[18]. While the direct use of measured input data may rightfully be regarded advantageously, a linearized analysis capability precludes exploration of such important matters as large-signal transient response, thermal sensitivity, distortion, and the like. Moreover, two port analyses render impossible a solution of the critically important problem of gauging circuit response sensitivity to the physical characteristics of both transistors and the monolithic fabrication process.

Second, COMPACT is restricted to the analysis of circuits having no more than 14 nodes. While this limitation can be obviated, it is cumbersome to do so and requires unreasonably imaginative modeling expertise.

Finally, COMPACT provides no information in regard to either the quiescent operating levels or the bias stability of simulated networks. This situation is a serious drawback since the desired bias solution for a wideband amplifier often establishes the appropriate small-signal parameter values commensurate with realization of a stipulated frequency response.

4.0 MBJT ELECTRICAL NOISE[20]

Considerable insight into the physical characteristics of bipolar transistors can be gleaned from a careful investigation of the electrical noise voltage produced at the output of a simple small-signal common emitter amplifier. The investigation commences with the small-signal noise model shown in Figure 4-1. Only the case of low-frequency signals is considered in deference to a desire to minimize cumbersome algebraic manipulations. Moreover, the low-frequency assumption is pragmatic, owing to the fact that the useful bandwidth of the majority of commerically available broadband noise monitoring equipment is restricted to frequencies that are well below the gain-bandwidth product limitations of modern transistors.

In the model of Figure 4-1, thermal noises generated in the resistive regions of the base, emitter, and collector are simulated by current generators I_{RB}, I_{RE}, I_{RC}, and I_{RO}, whose mean square values are given by

$$\Delta f^{-1} I_{RB}^2 = 4kT/r_b, \tag{4-1}$$

$$\Delta f^{-1} I_{RE}^2 = 4kT/R_E, \tag{4-2}$$

$$\Delta f^{-1} I_{RC}^2 = 4kT/r_c , \tag{4-3}$$

$$\Delta f^{-1} I_{RO}^2 = 4kT/R_{CO}, \tag{4-4}$$

where T is absolute junction temperature, k is Boltzman's constant, Δf is noise bandwidth, and resistance symbols are defined in the figure. Shot noise in the base and collector is modeled by uncorrelated current sources, I_{BN} and I_{CN}, with

$$\Delta f^{-1} I_{BN}^2 = 2qI_B \tag{4-5}$$

and

$$\Delta f^{-1} I_{CN}^2 = 2qI_C, \tag{4-6}$$

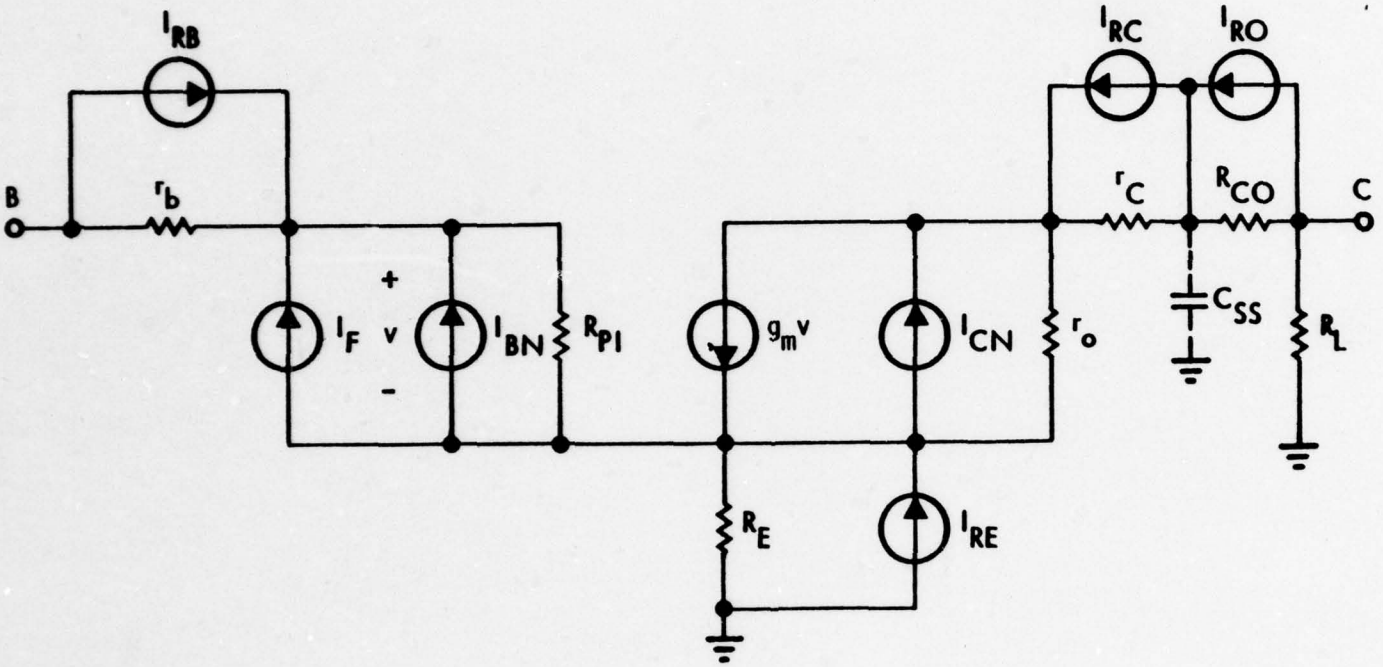

Figure 4-1 Small-Signal Bipolar Model for the Analysis of Electrical Noise

where q is electronic charge magnitude. Finally, flicker phenomena evolve from the presence of noise current I_F, wherein

$$\Delta f^{-1} I_F^2 = (\gamma I_B)\left(\frac{f_c}{f}\right)^d , \tag{4-7}$$

and γ, f_c, and d are empirical constants. In (4-5) through (4-7), I_B and I_C are quiescent base and collector currents, respectively.

Consider Figure 4-2 which depicts a simple AC schematic diagram of a common emitter amplifier driving noiseless load resistance R_L from a small voltage signal v_s having internal source resistance R_S. Voltage generator V_{SN} symbolizes thermal noise in the source and is defined by

$$\Delta f^{-1} V_{SN}^2 = 4kTR_S. \tag{4-8}$$

For noise analysis purposes, it is often convenient to represent the configuration of Figure 4-2 in any one of three distinctive ways. First, by replacing the transistor with the noise model of Figure 4-1, it is possible to refer the total qutput noise voltage, say V_{LN}, (due to both device and signal noise sources) to the input circuit so that the device in question is reduced to an ideal noiseless entity. If the referred input noise voltage is V_{iN}, as suggested in Figure 4-3a,

$$V_{iN} = \frac{V_{iN}}{A_0} , \tag{4-9}$$

where A_0 is the voltage gain magnitude. Alternatively, Figure 4-3b purports the existence of an input reference noise current, I_{iN}, such that

$$I_{iN} = \frac{V_{LN}}{R_{iN}} \tag{4-10}$$

where

$$R_{iN} = R_S A_0. \tag{4-11}$$

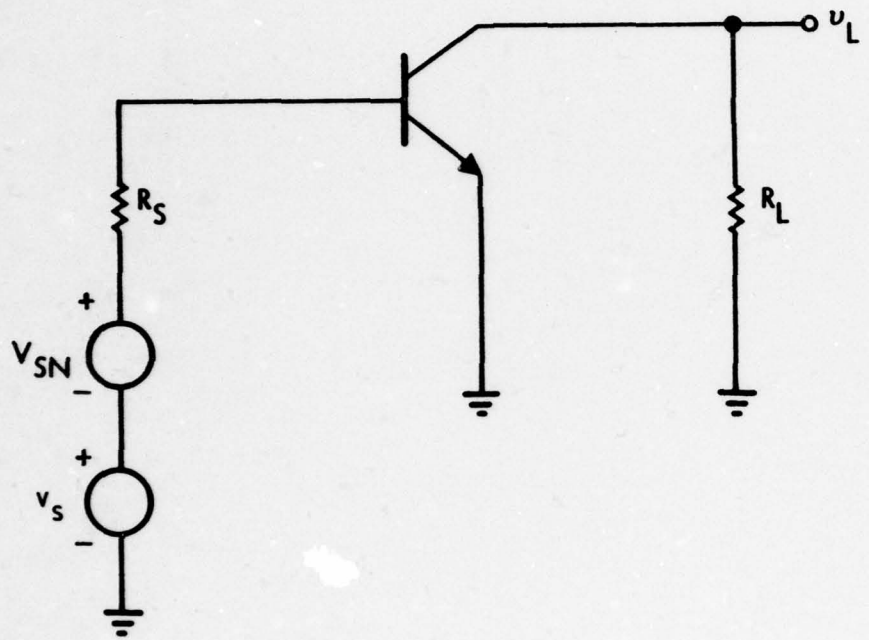

Figure 4-2 AC Schematic Diagram of Common-Emitter Amplifier Studied in Noise Investigation

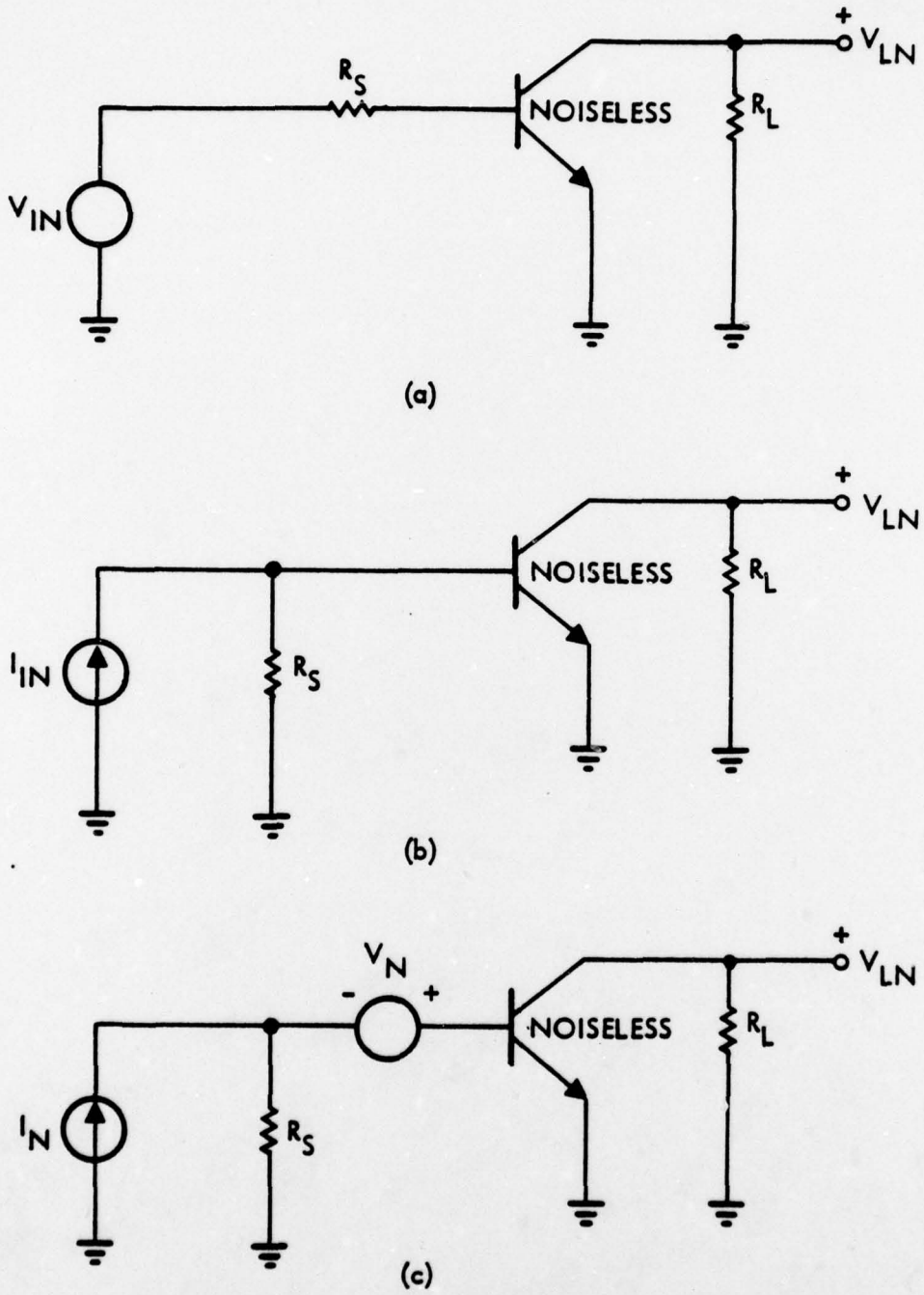

Figure 4-3 Circuits Used to Define (a) Reference Input Noise Voltage, (b) Reference Input Noise Current, (c) Equivalent Input Noise Voltage and Noise Current.

In all circuits, R_L is noisless, and noise due to R_S is absorbed into V_{iN} and I_{iN}.

A third representation is suggested by Figure 4-3c, in which V_N and I_N are termed the equivalent input noise voltage and equivalent input noise current, respectively. It is clear that

$$\left.\begin{aligned} V_N &= \underset{R_S \to 0}{\text{Lim}}(V_{iN}) \\ I_N &= \underset{R_S \to \infty}{\text{Lim}}(I_{iN}) \end{aligned}\right\} . \tag{4-12}$$

Observe that while V_{iN} and I_{iN} are noise performance measures of the entire network composed of device and external signal source, V_N, and I_N are independent of source noise. Consequently, (4-13) constitutes noise performance barometers of the bipolar device alone.

Finally, the noise figure, F, is often used to characterize the noise properties of an active network. By definition, F is the ratio of total mean-square output noise voltage to the mean-square output noise voltage generated solely by the noisy source termination. With reference to the preceding symbology,

$$F = \frac{V_{LN}^2}{(A_O V_{SN})^2} = \frac{V_{iN}^2}{4kTR_S \Delta f} . \tag{4-13}$$

Note that the noise figure specification compares the amplifier contribution to net output noise to the noise presented at the output port by the signal source alone. It follows that an ideal noiseless amplifier has F = 1.

Generalized expressions for V_{in}, I_{in}, V_N, I_N, and F can be developed upon replacement of the transistor of Figure 4-2 by the model shown in Figure 4-1. Despite the fact that a computer-based numerical evaluation of these noise parameters constitutes a trivial task, these expressions prove to be inordinately cumbersome unless a few simplifying approximations are invoked. Accordingly, let the forward gain be sufficiently large to render the contribution of I_{CN}, I_{RC}, and I_{RO} to total output noise inconsequentially small. Furthermore, let R_E be small enough to enable neglect of its contribution to output noise. The resultant

approximate model for noise analysis is shown in Figure 4-4. By allowing noise currents I_F and I_{BN} to shunt ground and internal base ports, as opposed to intrinsic emitter and internal base ports, the voltage drops, $I_{SN}R_E$ and $I_{LN}R_E$, are tacitly presumed to be much smaller than v and the drop across r_o, respectively.

Assuming that the noise sources in Figure 4-4 are uncorrelated, and recalling that A_O is the magnitude of voltage gain V_{LN}/V_{SN}, it is a simple matter to verify that the mean square output noise voltage is

$$V_{LN}^2 = A_O^2 \left\{ V_{SN}^2 + I_{RB}^2 (r_b{}^2)^2 + (I_{BN}^2 + I_F^2)(r_b + R_S)^2 \right\} . \tag{4-14}$$

Then from (4-1) through (4-7), the reference input noise voltage derives from

$$(4kT\Delta f)^{-1/2} V_{iN} = \left\{ R_S + r_b + \frac{R_S + r_b)^2}{2R_Q} \left(1 + \frac{\sigma}{2f^d}\right) \right\}^{1/2} \tag{4-15}$$

where

$$R_Q \triangleq \frac{kT}{qI_B} \tag{4-16}$$

$$\sigma \triangleq \frac{\gamma f_c{}^d}{q} . \tag{4-17}$$

It follows from (4-12) and (4-13) that the equivalent input noise voltage is determined from

$$(4kT\Delta f)^{-1/2} V_N = r_b \left\{ 1 + \left[\frac{r_b}{2R_Q}\right]\left[1 + \frac{\sigma}{2f^d}\right] \right\}^{1/2} \tag{4-18}$$

while the noise figure is

$$F = 1 + \frac{r_b}{R_S} + \frac{(R_S + r_b)^2}{2R_Q R_S} \left(1 + \frac{\sigma}{2f^d}\right). \tag{4-19}$$

Finally, (4-10) through (4-12) give, as the reference input and equivalent input noise current,

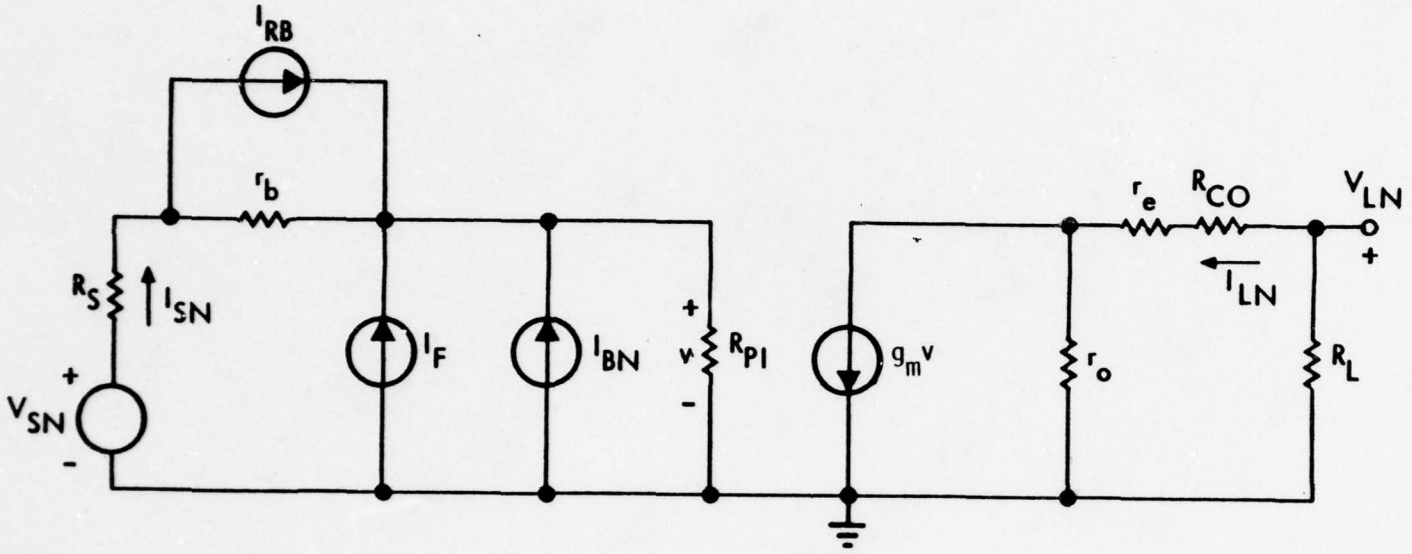

Figure 4-4 Approximate Model for Common Emitter Noise Analysis

$$I_{in} = \left(\frac{4kTF\Delta f}{R_S}\right)^{1/2} \tag{4-20}$$

and

$$(4kT\Delta f)^{1/2} I_N = \left[\frac{1 + \frac{\sigma}{2f^d}}{2R_Q}\right]^{1/2} . \tag{4-21}$$

It is of interest to interpret the foregoing results for the special cases of a voltage amplifier and a current amplifier. For the voltage amplifier case, in which R_S is a small source resistance, notice that the effective base resistance is a primary source of noise contamination. In particular, (4-18) shows that V_N, which in effect creates a noise-induced offset voltage at the base of a common emitter amplifier, vanishes if r_b is zero. If the transistor is indeed designed to offer minimal effective base resistance, (4-15) confirms that the reference input noise voltage, which superimposes directly with the externally applied signal source, is largely due to thermal noise in the small source resistance, except possibly at very low signal frequencies. Minimization of low frequency noise due to flicker phenomena is accomplished by maintaining large R_Q which, by (4-16), requires appropriately low quiescent base current. Implicit in the last assertion is the desirability of large DC beta. A large h_{FE} allows for the desired realization of small I_B, without incurring appreciable penalties in regard to output current compliance in the considered amplifier.

As might be anticipated, base resistance is not a crucial factor in the noise performance of an amplifier driven by a current source. For very large R_S, both (4-19) and (4-21) suggest that flicker noise is an unavoidable problem at low source signal frequencies. The degradation of amplifier performance due to flicker phenomena can, as in the case of a voltage source, be minimized by choosing a suitably small quiescent base current.

It is interesting to note that the noise figure-versus-source resistance curve displays a minimum at a source resistance value, say R_{SN}, which can be determined by setting the derivative, (dF/dR_S), to zero. It turns out that

$$R_{SN} = (R_{BO} + R_{BB}/K_B)\left\{1 + \frac{2R_Q/r_b}{1 + \sigma/2f^d}\right\}^{1/2}, \qquad (4\text{-}22)$$

which is identically the ratio, V_N/I_N.

Two important facts must be brought to light in conjunction with (4-22). First, noise figure minimization does not necessarily give rise to superior low noise performance of an amplifier. A minimum noise figure merely implies that the component of output noise due solely to the active device is minimal in comparison to the inevitable output signal contamination resulting from the amplified thermal noise in the source. Hence, large output noise voltages can be present in spite of low noise figure, if the source resistance is large.

The second point to be made is that (4-22) or, more meaningfully, the nature of ratio V_N/I_N alludes to a measurement procedure for effective base resistance. Observe that for very small signal frequencies, V_N/I_N converges toward r_b. This convergence is effected even more efficiently if in addition to subjecting the test transistor to low signal frequencies, the device is biased at large base currents (small R_Q). In implementing a large bias current, however, care must be exercised to ensure that I_B is not so large as to deliver emitter crowding-induced attenutation of the active component of net effective base resistance.

5.0 PARASITIC ENERGY STORAGE

The performance of a monolithic wideband analog circuit or high speed nonlinear circuit is often limited by the presence of on-chip parasitic energy storances, as opposed to limitations incurred by electrical phenomena intrinsic to the proposed circuit design. This state of affairs is especially true if extreme care has been exercised to ensure an optimal mathematical realization of a required circuit. In short, the presence of on-chip parasitics becomes progressively more significant as the design and synthesis procedures are made to produce circuit realizations that progressively approach an idealized structure.

There are primarily three types of on-chip parasitics that must be confronted in a circuit design venture. The first might be termed nodal coupling, which includes the deleterious effects of both electircal coupling between pairs of on-chip signal lines and electrical coupling between pairs of pads to which input signals are injected. The second type of parasitic is substrate coupling, which is signal attentuation caused by capacitive linkage between ground and transistor collectors and ground and passive elements fabricated monolithically. Finally, there is reactive coupling associated with the flux linkages of adjacent on-chip inductors.

As of this date, no unified theory underlying either the modeling of monolithic parasitics or the minimization of their cognate effects on required circuit specifications has evolved. Nevertheless, considerable experimental effort has been expended to measure on-chip energy storage parameters[19]. These endeavors have permitted various sorts of computations which, in turn, are used to formulate layout guidelines for individualized circuits.

5.1 Nodal Coupling

Four types of nodal coupling calculations have been performed for the OAT fabricaton process. First, the anticipated isolation between adjacent lines carrying single-ended signals has been simulated. It is shown that about 20dB of isolation is plausible at 1 GHz. Second, the anticipated isolation between adjacent pairs of lines carrying double-ended (balanced) signals has been investigated, and it is shown that better than 190dB of isolation is plausible. This inordinately large isolation magnitude infers that in a circuit realization, the overall isolation is determined almost exclusively by either the isolation characteristics of adjacent pads to which input signals are injected or the isolation limits imposed by the nature of the circuit undergoing design. The third analysis is offered in an attempt to bracket the extent of pad-to-pad isolation that can reasonably be expected at chip input. It is shown that about 60dB is feasible at 1 GHz. This figure is likely to be reduced by 10-15dB when the isolation characteristics of an optimized single-to-double ended converter are considered. Data for such a converter are not available.

Finally, the effects of imbalances in differential signal lines are addressed in the fourth analysis. It is shown that as much as 10%-to-15% differences in corresponding parameters in the differential signal drives incur negligible isolation degradation.

The parameters utilized in all models exercised on the computer derive from the following specifications or worst case presumptions.

1). Signal lines are 150 mils long and 10 microns wide. Shorter, narrower lines incur enhanced isolation capability.

2). The substrate is 15 mils thick and has a nominal resistivity of 20 ohm-centimeters.

3). Signal lines are separated by 15 mils.

5.1.1 Single-Ended Configuration

The model pertinent to adjacent lines driven by traditional single-ended signals is shown in Figure 5-1. In this model,

$$C_1 = C_2 \approx 1.2\text{pF}$$

$$R_1 = R_2 \approx 75 \text{ ohms}$$

$$R_3 \approx 13 \text{ ohms}.$$

Figure 5-2 displays the isolation characteristics versus frequency, DBI versus f, where

$$\text{DBI} \triangleq -20\text{Log}\left|V_{OUT}/V_{IN}\right|. \qquad (5\text{-}1)$$

Observe that 320 MHz is the upper frequency limit of a reasonable expectation of 50dB RF switch isolation.

5.1.2 Double-Ended (Balanced) Topology

Figure 5-3 depcits the model, and Figure 5-4 displays results. Model parameters are

$$C_1 = C_2 = C_3 = C_4 \approx 1.2\text{pF}$$

$$R_1 = R_2 = R_3 = R_4 = R_5 = R_6 \approx 0.55 \text{ ohms}$$

$$R_7 = R_8 = R_9 = R_{10} = 75 \text{ ohms}.$$

The results strongly imply that on-chip isolation does not determine overall circuit/signal isolation. Instead, overall isolation is fixed by the isolation parameters associated by the circuits required to convert from single-ended-to-double-ended mode of transmission.

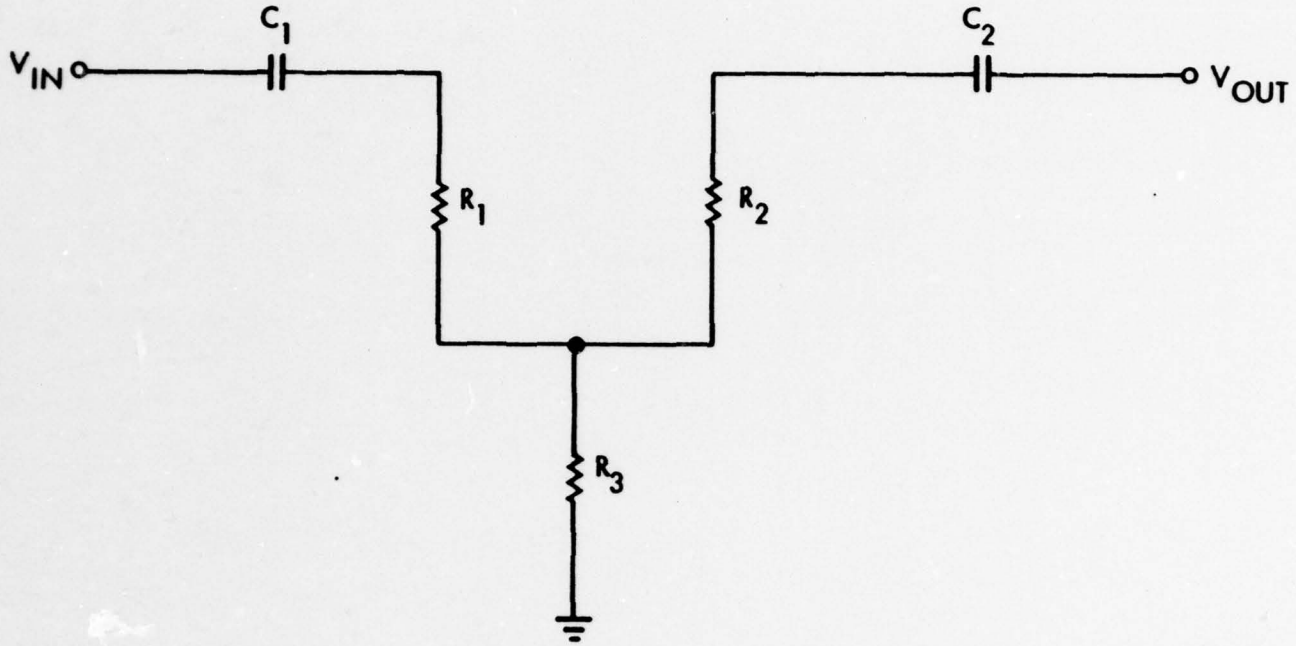

Figure 5-1 Electrical Model for Single-Ended Isolation Analysis
Signals are carried "perpendicular" to page at V_{IN} and V_{OUT}, respectively.

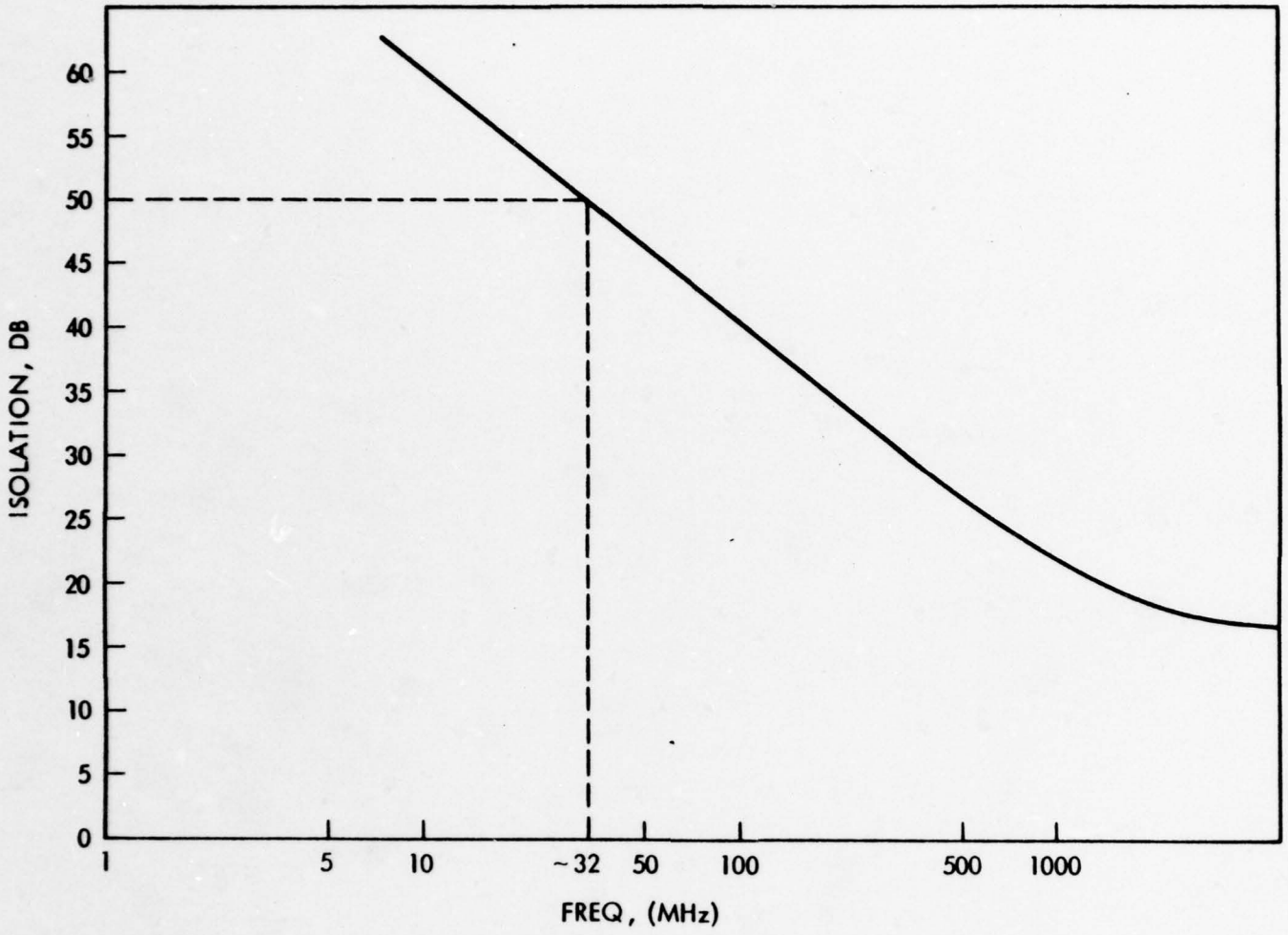

Figure 5-2 Single-Ended Isolation Characteristics

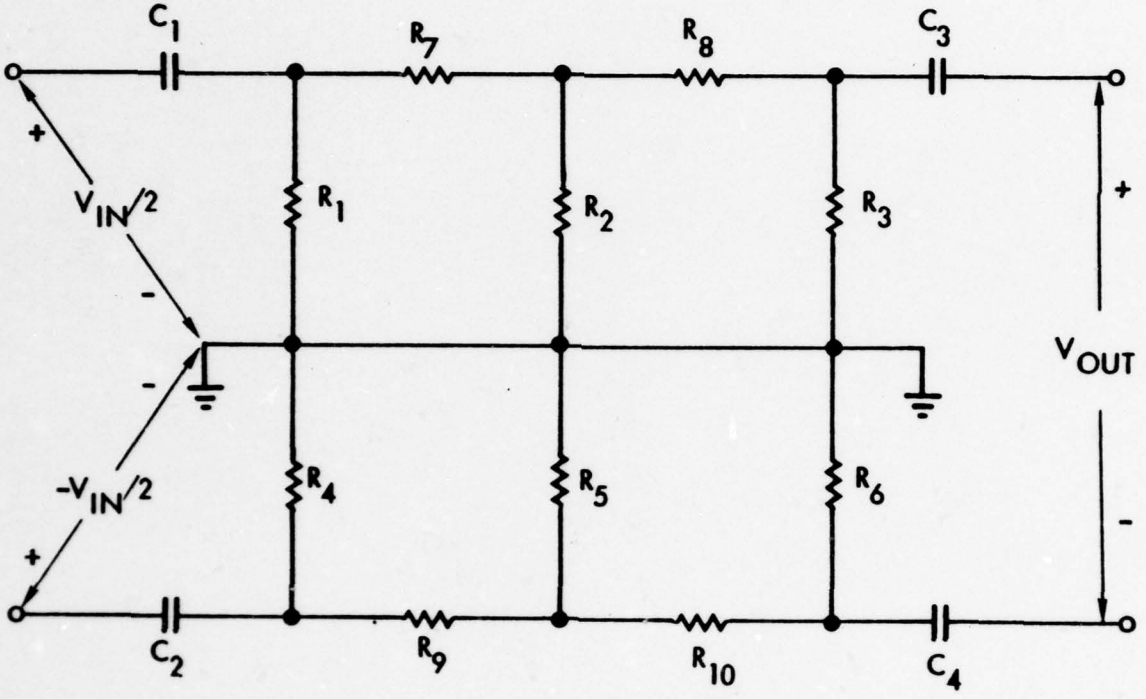

Figure 5-3 Electrical Model for Balanced Isolation Analysis

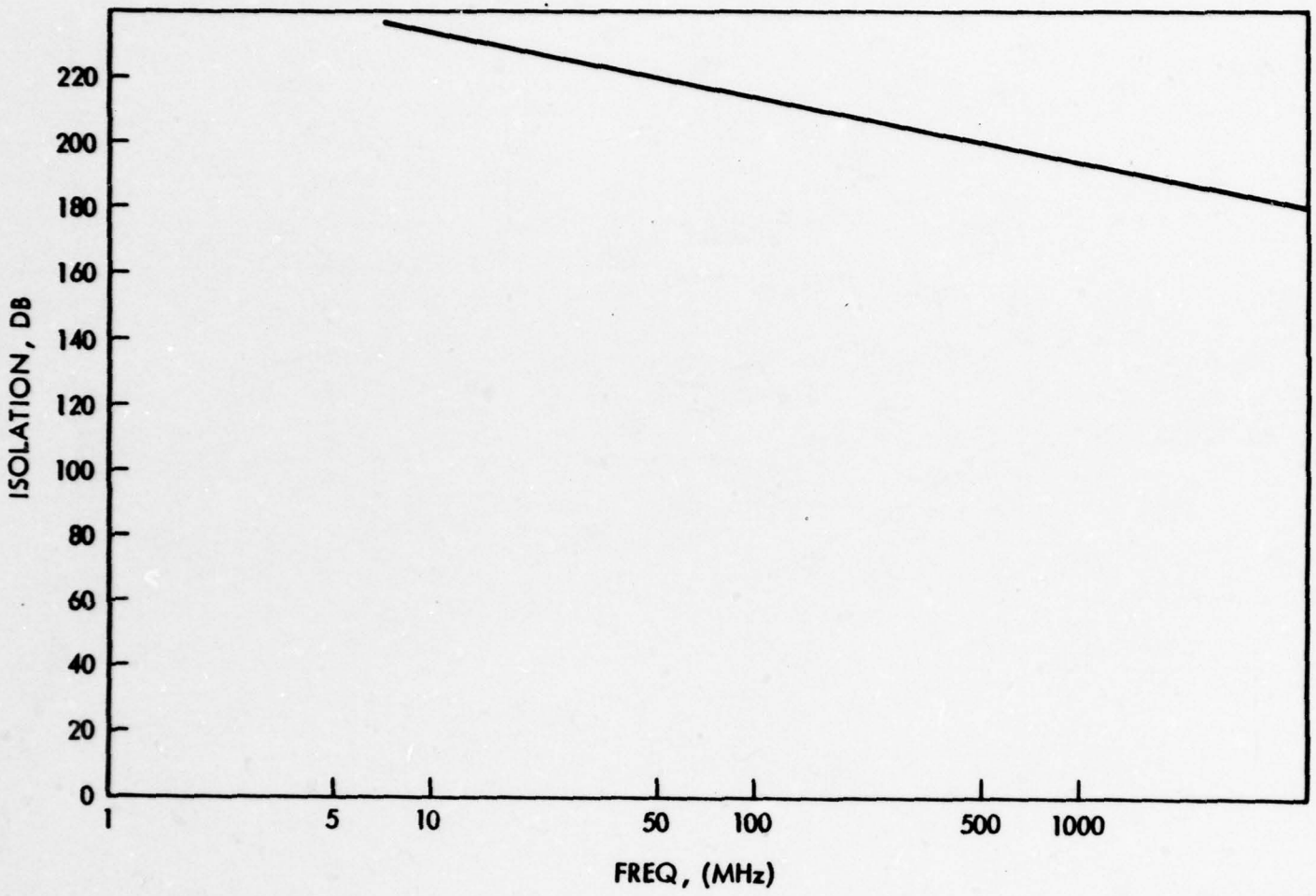

Figure 5-4 Isolation Characteristics for Balanced Signal Lines

5.1.3 Pad Isolation

The electrical model germane to the simulation of isolation characteristics at the input signal pads is shown in Figure 5-5. Signals are carried along lines which pass perpendicularly to the page at terminals labeled "SIGNAL 1" and "SIGNAL 2." A grounded isolation pad is inserted between the two signal pads. Inductance L (0.1 nhy) accounts for parasitic grounding reactance. The model parameters are

$$C_{CS} \approx 0.3pF$$

$$R_1 \approx 950 \text{ ohms}$$

$$R_S \approx 50 \text{ ohms.}$$

The numbers assume a pad width of 4 mils and 10 mils of pad separation.

The isolation response is depicted in Figure 5-6. This plot is useful in that one can expect the required input converter to have similar characteristics with perhaps 10-15dB of additional degradation.

5.1.4 Double-Ended Imbalances

The models of both Figures 5-3 and 5-5 were re-exercised on the computer with mirrored parameters imbalanced by random percentages of as much as 15%. This study was performed to ascertain the amount of isolation degradation that might be incurred as a direct result of the impossibility of achieving perfect matching among apparently homologous integrated circuit parameters. The degradation in the simulated characteristics of Figure 5-5 and 5-6 were found to be less than 0.9dB at all frequencies.

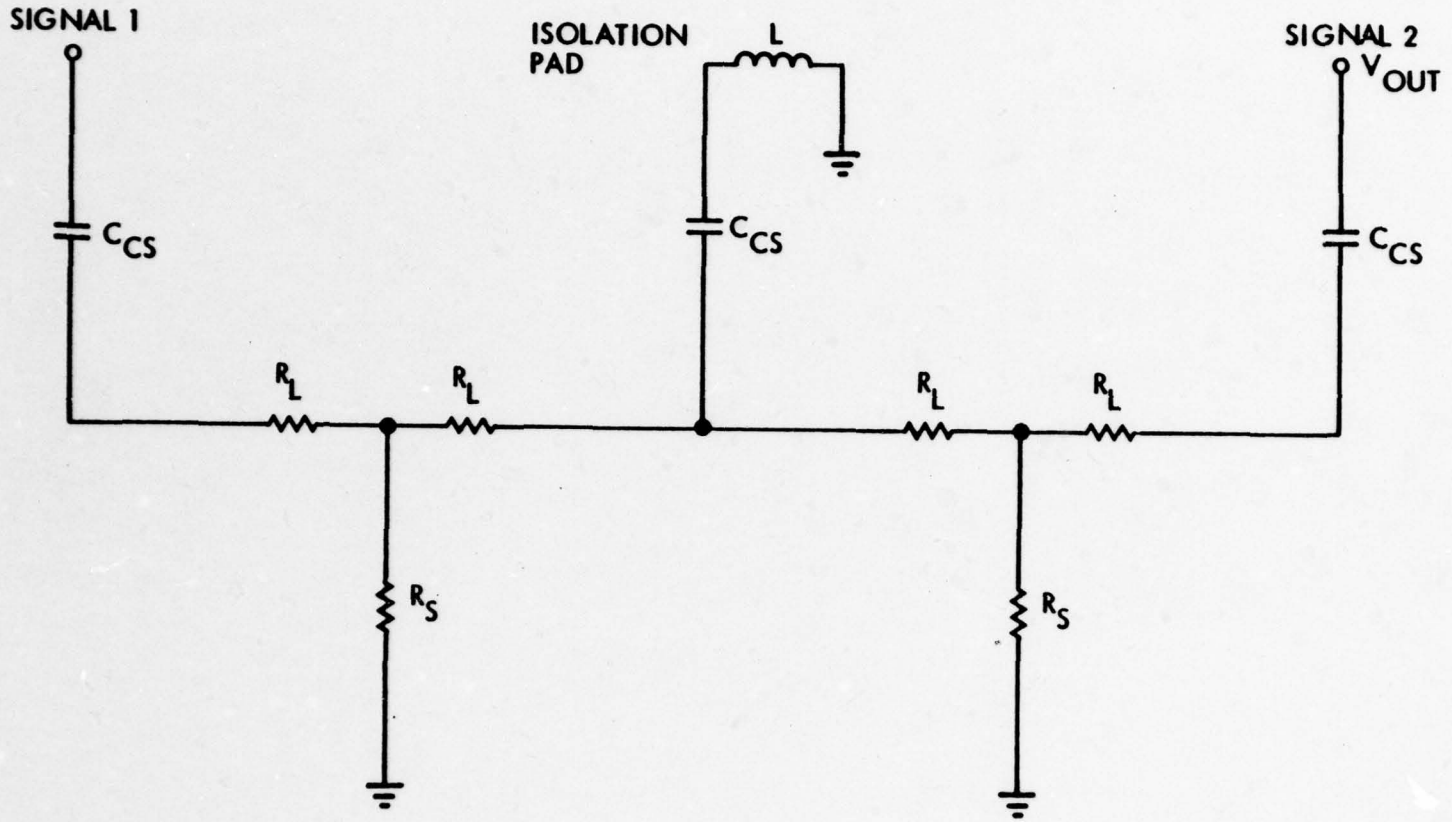

Figure 5-5 Electrical Model of Isolation Structure at Input Signal Pads of Chip

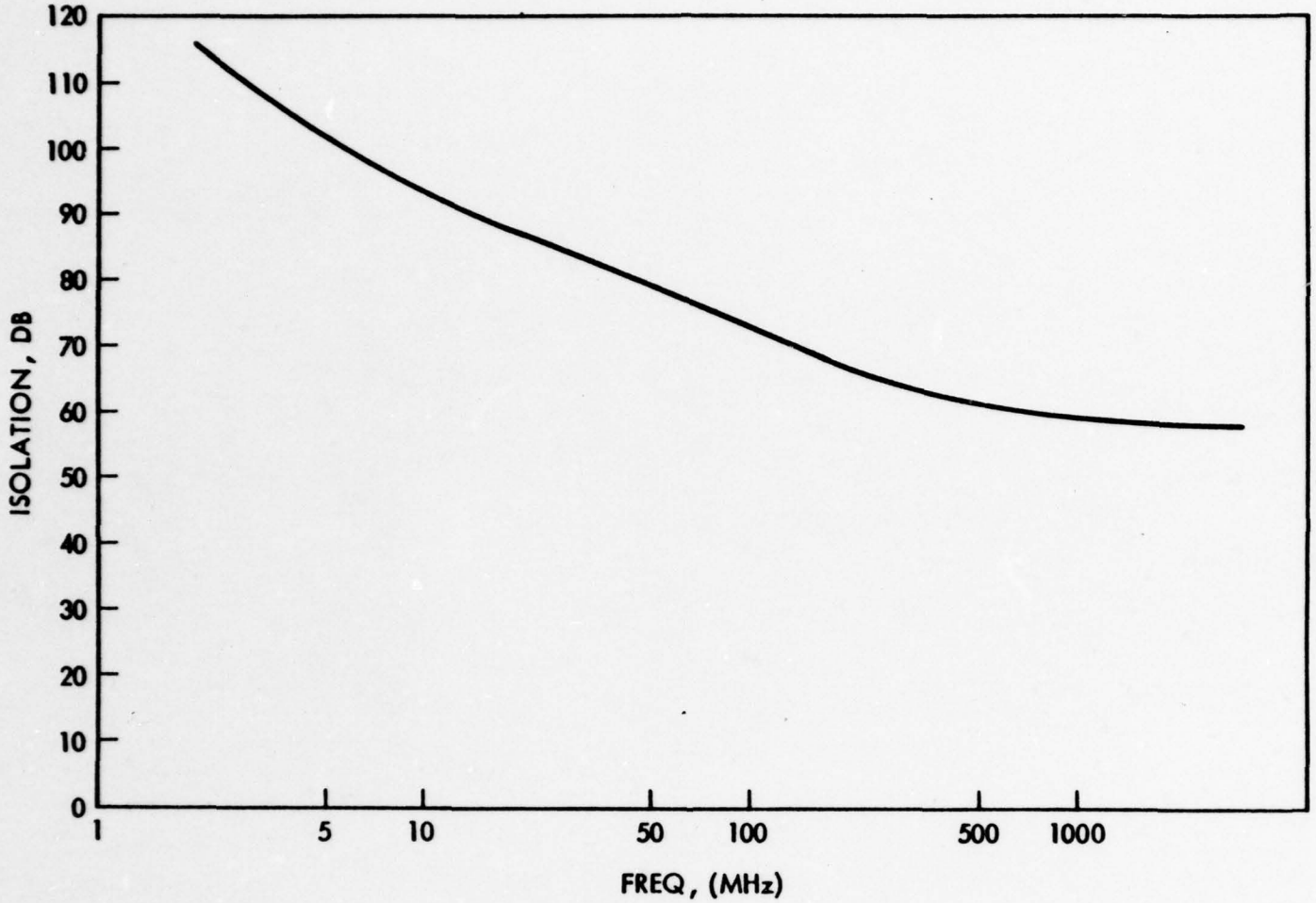

Figure 5-6 Pad Isolation Characteristics with Grounded Pad Between Signal Inputs

5.1.5 Conclusions

This preliminary study leads to the belief that 45-to-50dB of RF circuit isolation is achievable with OAT RFLSI at 1 GHz. The quoted isolation presumes that an acceptable single-ended to differential signal converter can be designed to ensure realizability of isolation specifications. Indeed, the overall isolation of a differential RF circuit appears to be limited almost exclusively by the combination of isolation degradations incurred at both the signal input pads and converter.

5.2 On-Chip Inductance

As discussed in Section 2.3, the interstage matching networks are strongly conducive to the realization of wideband amplification networks. For monolithic circuits, this situation is unfortunate since invariably, inductive components are required to achieve proper interstage impedance matching.

In the OAT process, inductors are realized by a flat spiral coil of first level metal. As shown in Figure 5-7, an electrical connection is made to one terminal of the coil by means of first level metal, while the connection to the other coil terminal is made by second level metal underneath the spiral of first level metal. First level metal sits on 1.1 microns of field oxide over an epitaxial layer on the substrate. The two levels of metal are separated by a deposited film of silicon dioxide dielectric. Electrical contact is made through via holes etched in the dielectric.

There are a number of parasitics associated with an integrated circuit inductor. Perhaps the most serious is nonzero resistivity of both first and second level metal. For first level metal, the average resistivity is 0.06 ohms per square, while second level metal is characterized by a resistivity of approximately 0.04 ohms per square. The upshot of the matter is that coil quality factor in the neighborhood of 1 GHz are rarely above five and typically, they are less than three. Moreover, eddy current losses in the epitaxial layer and in the substrate has the effect of generating an additional resistance in series with

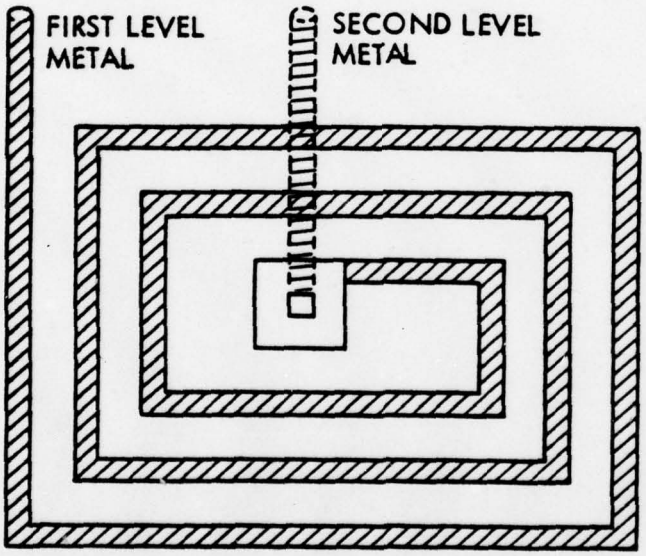

Figure 5-7 Symbolic Representation of Integrated Spiral Inductor

the coil. The resistance precipated by parasitic eddy currents is frequency dependent and causes enhanced degradation in quality factor.

Parasitic signal coupling is realized through mutual inductance among the various turns of the spiral, capacitance between adjacent turns, and most predominantly, capacitance from the various spiral turns to the substrate. The latter capacitance, which is modeled in Section 2.3.2 as the lumped entity, C/2, is proportional to the net area encumbered by the spiral. Since large inductance demands large area, this coupling parasitic imposes an upper limit on the practical inductance value that can be synthesized for use in circuits subjected to prescribed signal frequency environments. At 1 GHz, a typical upper limit to inductance is in the range of 10-15 nanoheneries. For fixed inductance, a practical upper frequency limit is the parameter, $\sqrt{\omega_o \omega_p}$, as discussed in Section 2.3.2.

Experience has shown that the foregoing parasitics incur a substantial error between measured inductance and the inductance predicted by theoretical formulas which relate inductance to premeability, number of turns, and geometrical factors[21]. For the OAT process, cognate experimental evidence infers that these theoretical equations can be utilized, provided that the premeability of the silicon dioxide dielectric is multiplied by a factor of approximately 2.2.

5.3 On-Chip Capacitance

Three types of capacitors are available in the OAT process; namely, the metal-oxide metal or MOM capacitor, the metal-oxide-silicon (MOS) capacitor, and the junction depletion capacitor.

The MOM capacitor is fabricated by laying first level metal on a field oxide, depositing silicon dioxide dielectric, and thence depositing second level metal. The resultant capacitive yield is of the order of 0.29 picofarads per square mil. The MOM capacitor is characterized by very low series resistance, but unfortunately, it has large capacitive coupling to either the substrate or to the diffused layer under the MOM. Typically, the parasitic capacitance is approximately 60% of the total desired MOM capacitance.

The MOS capacitance is formed of first or second level metal and silicon, with oxide dielectric. An oxide dielectric thickness of 1.1 microns provides a capacitance of 0.02 picofarads per square mil, while the deep collector oxide dielectric of 0.7 micron thickness delivers 0.03 picofarads per square mil. Since one side of the MOS capacitor is a diffused layer, large series resistance coupling is evidenced. The amount of coupling is dependent on layout and contact goemetry at the diffused layer. Additionally, parasitic voltage-dependent capacitive coupling is evidenced between the diffused layer and substrate.

The junction capacitance is voltage dependent, has large series resistance on both sides of the element and generally exhibits voltage breakdown. A typical isolation-to-buried layer junction capacitance gives 0.7 picofarads per square mil at zero terminal voltage, with a maximum operating voltage of about 7 volts. Parasitic capacitive coupling to the substrate occurs at the buried layer side.

6.0 ANALOG MULTIPLIER CIRCUITS

An ideal analog multiplier is a circuit whose output voltage or current is linearly proportional to the product of two applied input signals. All practical multipliers suffer from one or more of at least six shortcomings[22].

1). The output is, in addition to being dependent on the product of inputs, nonlinearly dependent on one or both of the inputs.

2). The proportionality constant, K, in the idealized characteristic equation,

OUTPUT = K(PRODUCT OF TWO INPUTS) is frequency dependent. (6-1)

3). The output is not suppressed to zero when one of the two inputs is a null excitation.

4). Constant K in (6-1) varies with temperature and quiescent supply voltages.

5). An equivalent quiescent offset is generated with respect to one or both inputs.

6). An output quiescent offset voltage is produced.

Of the numerous available types of analog multipliers[23], the so-called variable transconductance multiplier appears best suited to very high frequency operation. This multiplier exploits the exponential volt-ampere characteristics of bipolar transistor junctions and uses pairs of transistors connected as differential amplifiers. The variable transconductance multiplier conforms reasonably to (6-1) when the input signal magnitudes are small, but for large signal inputs, significant departures from ideal operation are observable. The immediate effect of non-ideal operation is the production of spurious frequencies; i.e., frequencies other than the upper and lower sidebands associated with the Fourier spectrum of each of the two input signals. The criticality of minimizing spurious frequencies in a GPS receiver justifies an in-depth analysis of the potential sources of multiplier distortion.

6.1 DC Analysis

6.1.1 Single Transistor

Consider first a single transistor with emitter degeneration resistance, as shown in Figure 6-1. The collector current (I_C) is approximately given by

$$I_C = I_S(\varepsilon^{V_{BE}/v_T}) \tag{6-2}$$

over several orders of current magnitude. The emitter current (I_E) is

$$I_E = I_C + \frac{I_C}{\beta} = I_C(\frac{\beta + 1}{\beta})$$

which is approximately equal to the collector current (I_C) for large values of quiescent current transfer ratio, β. Thus

$$I_E \simeq I_S\varepsilon^{V_{BE}/v_T}\ , \tag{6-3}$$

where

$$V_{BE} = V_1 - I_E R_E. \tag{6-4}$$

Substituting for V_{BE} in (6-3),

$$I_E \simeq I_S\varepsilon^{(V_1 - I_E R_E)/v_T}, \tag{6-5}$$

which can be expanded in a Taylor series expansion about the quiescent base-emitter voltage, say V_Q. Namely,

$$I_E(V_Q + v) = I_{EQ} + v\frac{dI_E}{dV_{BE}}\Big|_{V_{BE} = V_Q} + \frac{v^2}{2!}\frac{d^2I_E}{dV_{BE}^2}\Big|_{V_{BE} = V_Q} + \frac{v^3}{3!}\frac{d^3I_E}{dV_{BE}^3}\Big|_{V_{BE} = V_Q} + \cdots \tag{6-6}$$

The coefficient of the linear term is

$$\frac{dI_E}{dV_{BE}} = \frac{(\frac{I_S}{v_T})\varepsilon^{(v - R_E I_E)/v_T}}{\left[1 + R_E(\frac{I_S}{v_T})\varepsilon^{(v_T - R_E I_E/v_T)}\right]} \tag{6-7}$$

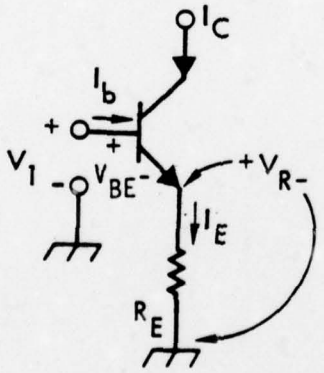

Figure 6-1 Single Transistor With Emitter Degeneration Resistance

and at the quiescent operating point:

$$\frac{dI_E}{dV'_{BE}}\Big|_{V_{BE}} = V_Q = \left[\frac{g_m}{1 + R_E g_m}\right] = g'_m = A_1 \qquad (6\text{-}8)$$

where

$$g_m = \left(\frac{I_S}{v_T}\right)\epsilon^{(V_Q - RI_{EQ})/v_T} = \left(\frac{I_{EQ}}{v_T}\right) . \qquad (6\text{-}9)$$

Equation (6-8) exudes the familiar emitter degeneration of forward transconductance g_m.

A few of the higher order terms are

$$\frac{d^2I_E}{dV^2_{BE}}\Big|_{V_{BE}} = V''_Q = \left[\frac{g_m}{v_T(1 + g_m R_E)^3}\right] = A_2; \qquad (6\text{-}10)$$

$$\frac{d^3I_E}{dV^3_{BE}}\Big|_{V_{BE}} = V'''_Q = \left[\frac{g_m(1 - 2g_m R_E)}{v_T^2(1 + g_m R_E)^5}\right] = A_3; \qquad (6\text{-}11)$$

$$\frac{d^4I_E}{dV^4_{BE}}\Big|_{V_{BE}} = V^{(4)}_Q = \left[\frac{g_m(1 - 8g_m R_E + 6(g_m R_E)^2}{v_T^3(1 + g_m R_E)^7}\right] = A_4; \qquad (6\text{-}12)$$

$$\frac{d^5I_E}{dV^5_{BE}}\Big|_{V_{BE}} = V^{(5)}_Q = \left[\frac{g_m(1 - 22g_m R_E + 58(g_m R_E)^2 - 24(g_m R_E)^3}{v_T^4(1 + g_m R_E)^9}\right] = A_5. \qquad (6\text{-}13)$$

Note that if $g_m R_E >> 1$ g'_m the Taylor series is

$$I_E(V_Q + v) \approx \left\{I_{EQ} + \frac{v}{R_E} + \frac{v^2}{2Rv_T(g_m R)^2} - \frac{v^3}{3Rv_T^2(g_m R)^3}\right.$$

$$\left. + \frac{v^4}{4Rv_T^3(g_m R)^4} - \frac{v^5}{5Rv_T^4(g_m R)^5} + \ldots\right\} . \qquad (6\text{-}14)$$

If there is no emitter degeneration, $R_E = 0$, and the emitter current expansion is

$$I_E(V_Q + v) = \left[I_{EQ} + g_m v + \frac{I_{EQ} v^2}{2! v_T^2} + \frac{I_{EQ} v^3}{3! v_T^3} + \ldots \right] \tag{6-15}$$

$$= I_{EQ} \left[1 + (v/v_T) + \frac{(v/v_T)^2}{2!} + \frac{(v/v_T)^3}{3!} + \ldots \right] . \tag{6-16}$$

All of the derivatives are well behaved and these series are convergent for <u>all</u> values of v.

Note that for $v << v_T$ the series in (6-14) can be approximated by the linear term,

$$I_E(V_Q + v) \approx I_{EQ} + \frac{g_m v}{1 + g_m R_E} \quad ; \quad (v << v_T). \tag{6-17}$$

6.1.2 <u>Differential Pair</u>

Consider the differential configuration of Figure 6-2. The two input voltages can be decomposed into differential and common mode components:

$$\left.\begin{aligned} v_1 &= V_{CM} + v/2 \\ v_2 &= V_{CM} - v/2 \end{aligned}\right\} \quad ; \tag{6-18}$$

Thus, $v_1 - v_2 = v$. (6-19)

The Taylor series for I_1 and I_2 are easily written

$$\left.\begin{aligned} I_1(V_{CM} + v/2) &= I_Q + A_1(\tfrac{v}{2}) + \frac{A_2}{2!}(\tfrac{v}{2})^2 + \frac{A_3}{3!}(\tfrac{v}{2})^3 + \ldots \\ I_2(V_{CM} - v/2) &= I_Q - A_1(\tfrac{v}{2}) + \frac{A_2}{2!}(\tfrac{v}{2})^2 - \frac{A_3}{3!}(\tfrac{v}{2})^3 + \ldots \end{aligned}\right\} , \tag{6-20}$$

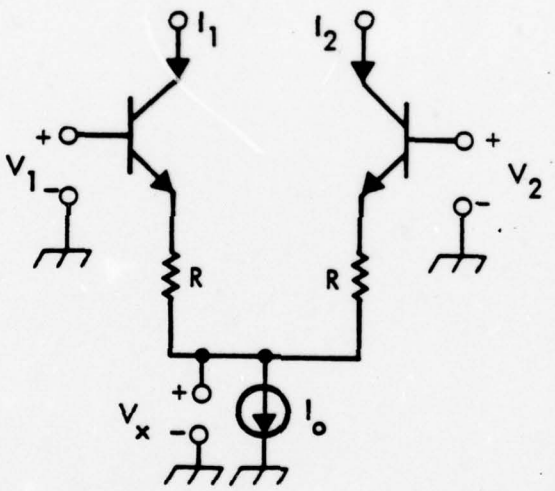

Figure 6-2 Differential Pair With Ideal Current Source

where the coefficients are the derivatives defined by (6-8) through (6-13). Subtracting equations (6-20) produces differential current,

$$(I_1 - I_2) = \left[A_1 v + 2\frac{A_3}{3!}\left(\frac{v}{2}\right)^3 + 2\frac{A_5}{5!}\left(\frac{v}{2}\right)^5 + \ldots\right] . \qquad (6\text{-}21)$$

For R = 0,

$$(I_1 - I_2) = I_0\left[(v/2v_T) + \frac{(v/2v_T)^3}{3!} + \frac{(v/2v_T)^5}{5!} + \ldots\right] \qquad (6\text{-}22)$$

while if $g_m R >> 1$,

$$(I_1 - I_2) \simeq \frac{2(v/2)}{R} - \frac{2(v/2)^3}{3Rv_T^2(g_mR)^3} - \frac{2(v/2)^5}{5Rv_T^4(g_mR)^5} - \ldots \qquad (6\text{-}23)$$

6.2 Circuit Realization

6.2.1 Basic Circuit

The basic transconductance multiplier of Figure 6-3 has three differential pairs. The inputs are

$$\left.\begin{aligned} V_{A1} &= V_A + v_a/2 \\ V_{A2} &= V_A - v_a/2 \\ V_{A1} - V_{A2} &= v_a \\ V_{B1} &= V_B + v_b/2 \\ V_{B2} &= V_B - v_b/2 \\ V_{B1} - V_{B2} &= v_b \end{aligned}\right\} . \qquad (6\text{-}24)$$

The differential current $(I_{A1} - I_{A2})$ can be written from (6-21) as

$$(I_{A1} - I_{A2}) = \left(\frac{v_a}{2}\right)\left[2A_1 + \frac{2A_3}{3!}\left(\frac{v_a}{2}\right)^2 + \frac{2A_5}{5!}\left(\frac{v_a}{2}\right)^4 + \ldots\right] . \qquad (6\text{-}25)$$

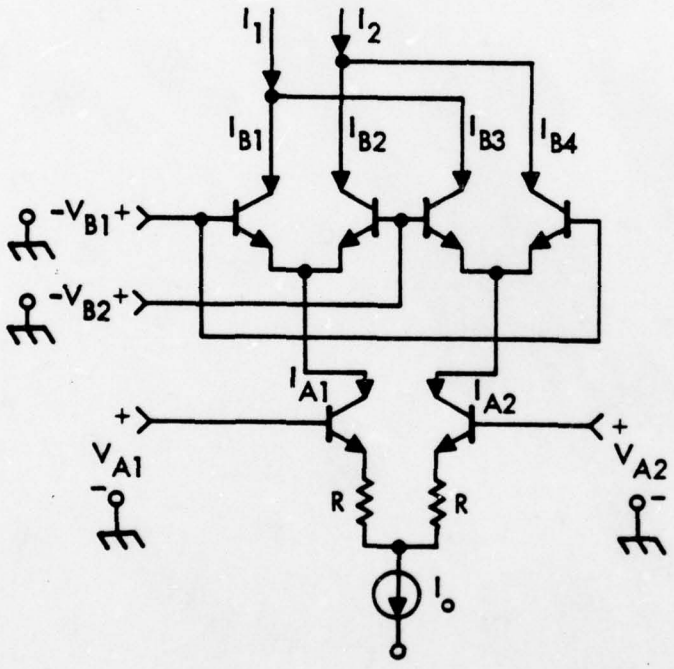

Figure 6-3 Simplified Schematic Diagram of Practical Multiplier

The output current $(I_1 - I_2)$ is given by

$$(I_1 - I_2) = (I_{B1} + I_{B3}) - (I_{B2} + I_{B4}) = (I_{B1} - I_{B2}) + (I_{B3} - I_{B4}) \quad (6\text{-}26)$$

and from (6-22)

$$(I_{B1} - I_{B2}) = I_{A1}\left[(v_b/2v_T) + \frac{(v_b/2v_T)^3}{3!} + \frac{(v_b/2v_T)^5}{5!} + \ldots\right]$$

$$(I_{B3} - I_{B4}) = I_{A2}\left[(-v_b/2v_T) + \frac{(-v_b/2v_T)^3}{3!} + \frac{(-v_b/2v_T)^5}{5!} + \ldots\right]. \quad (6\text{-}27)$$

Thus (6-26) becomes expressible as

$$(I_1 - I_2) = (I_{A1} - I_{A2})\left[(v_b/2v_T) + \frac{(v_b/2v_T)^3}{3!} + \frac{(v_b/2v_T)^5}{5!} + \ldots\right],$$

and factoring out $(v_b/2v_T)$,

$$(I_1 - I_2) = (I_{A1} - I_{A2})\left(\frac{v_b}{2v_T}\right)\left[1 + \frac{(v_b/2v_T)^2}{3!} + \frac{(v_b/2v_T)^4}{5!} + \ldots\right]. \quad (6\text{-}28)$$

Substituting for $(I_{A1} - I_{A2})$ from (6-25),

$$(I_1 - I_2) = \left(\frac{v_a}{2}\right)\left(\frac{v_b}{2}\right)\frac{1}{v_T}\left[1 + \frac{(v_b/2v_T)^2}{3!} + \frac{(v_b/2v_T)^4}{5!} + \ldots\right] \times$$

$$\left[2A_1 + \frac{2A_3}{3!}\left(\frac{v_a}{2}\right)^2 + \frac{2A_5}{5!}\left(\frac{v_a}{2}\right)^4 + \ldots\right]. \quad (6\text{-}29)$$

If $g_mR \gg 1$, the last result approximates as

$$(I_1 - I_2) \approx \frac{v_a v_b}{2Rv_T}\left[1 + \frac{(v_b/2v_T)^2}{3!} + \frac{(v_b/2v_T)^4}{5!} + \ldots\right] \times$$

$$\left[1 - \frac{(v_a/2v_T)^2}{3(g_mR)^3} - \frac{(v_a/2v_T)^4}{5(g_mR)^5} - \ldots\right] \quad (6\text{-}30)$$

and upon multiplication,

$$(I_1 - I_2) \approx \frac{v_a v_b}{2Rv_T}\left\{1 + \left(\frac{(v_b/2v_T)^2}{3!} - \frac{(v_a/2v_T)^2}{3(g_mR)^3}\right)\right.$$

$$\left. + \left(\frac{(v_b/2v_T)^4}{5!} - \frac{(v_b/2v_T)^2(v_a/2v_T)^2}{3!3(g_mR)^3} - \frac{(v_a/2v_T)^5}{5(g_mR)^5}\right) + \ldots\right\} \qquad (6\text{-}31)$$

For very small inputs ($v_a/v_T << 1$, $v_b/v_T << 1$) the higher order terms can be ignored, leaving

$$(I_1 - I_2) \approx \frac{v_a v_b}{2Rv_T}\,, \qquad (6\text{-}32)$$

which is the idealized form of multiplier output. Notice that if the inputs are time varying, it is impossible for the higher order terms to cancel out, because v_a and v_b are independent variables.

The higher order terms containing v_a can be decreased by making (g_mR) very large. The greatest contribution to high order outputs comes from terms involving v_b. Emitter degeneration cannot be used because the transconductance modulated by v_a causes performance degradation with respect to the higher order terms.

6.2.2 Preconditioned Signal Input

To correct for the nonlinearity caused by large v_b, a modification in the circuit is needed to precondition signal v_b, thereby neutralizing its nonlinear components. Consider the transconductance multiplier shown in Figure 6-4. In this circuit, v_b is converted to the current $(I_{D1} - I_{D2})$. Differential voltage $(v_1 - v_2)$ is then proportional to the log of I_{D1}/I_{D2}). The current $(I_1 - I_2)$ is proportional to the antilog of I_{D1}/I_{D2}, and hence proportional to $v_b$and v_a.

The emitter currents of $Q_1 - Q_4$ can be written

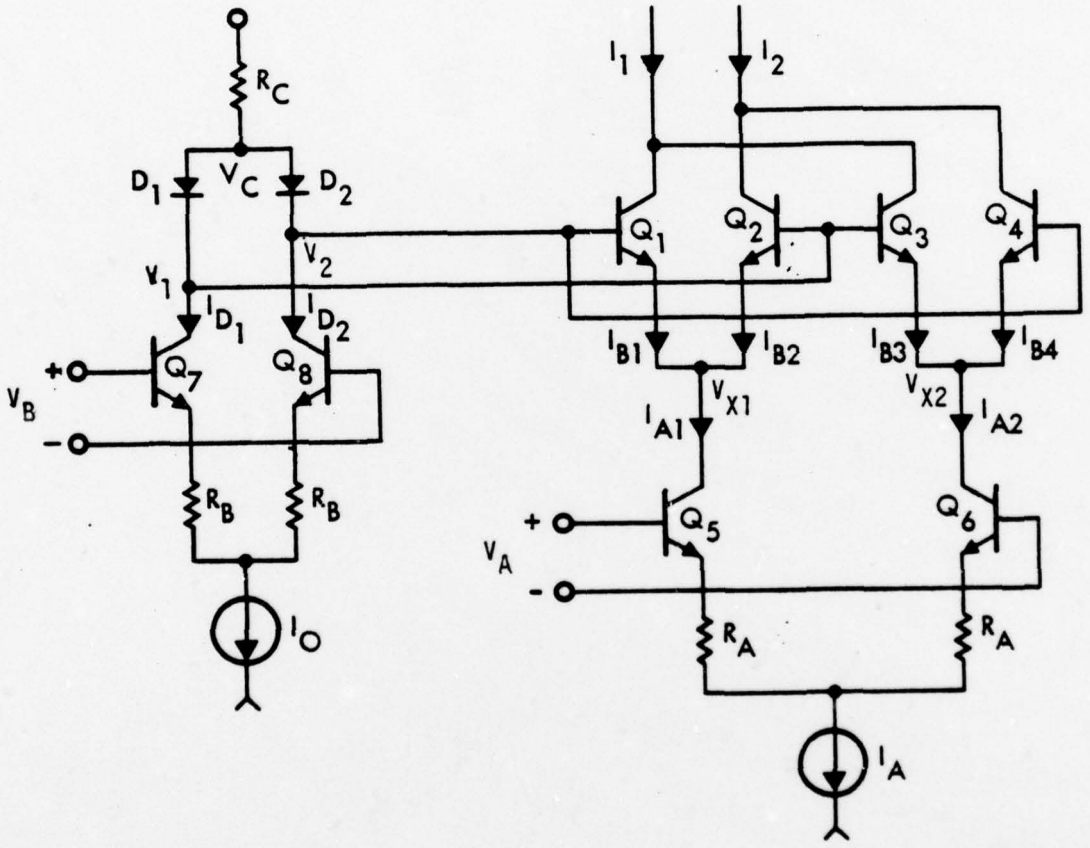

Figure 6-4 Multiplier with Diode Preconditioning Used to Neutralize Nonlinear Signal Inputs at Stage having no Emitter Degeneration

$$\left.\begin{aligned} I_{B1} &= I_S \varepsilon^{(v_2 - v_{x1})/v_T} \\ I_{B2} &= I_S \varepsilon^{(v_1 - v_{x1})/v_T} \\ I_{B3} &= I_S \varepsilon^{(v_1 - v_{x2})/v_T} \\ I_{B4} &= I_S \varepsilon^{(v_2 - v_{x2})/v_T} \end{aligned}\right\} \quad . \tag{6-33}$$

I_{A1} and I_{A2} can then be written

$$I_{A1} = I_{B1} + I_{B2} = I_S \left[\varepsilon^{-v_{x1}/v_T}\right]\left[\varepsilon^{v_1/v_T} + \varepsilon^{v_2/v_T}\right] \tag{6-34}$$

$$I_{A2} = I_{B3} + I_{B4} = I_S \left[\varepsilon^{-v_{x2}/v_T}\right]\left[\varepsilon^{v_1/v_T} + \varepsilon^{v_2/v_T}\right] . \tag{6-35}$$

The differential output current is

$$(I_1 - I_2) = (I_{B1} + I_{B3}) - (I_{B2} + I_{B4}) \tag{6-36}$$

$$= I_S\left[\varepsilon^{(v_2 - v_{x1})/v_T} + \varepsilon^{(v_1 - v_{x2})/v_T} - \varepsilon^{(v_1 - v_{x1})/v_T} + \varepsilon^{(v_2 - v_{x2})/v_T}\right] \tag{6-37}$$

$$= I_S\left[\varepsilon^{-v_{x1}/v_T}\right]\left[\varepsilon^{v_2/v_T} - \varepsilon^{v_1/v_T}\right] + I_S\left[\varepsilon^{-v_{x2}/v_T}\right]\left[\varepsilon^{v_1/v_T} - \varepsilon^{v_2/v_T}\right] . \tag{6-38}$$

But from (6-34) and (6-35),

$$I_S\left[\varepsilon^{-v_{x1}/v_T}\right] = \frac{I_{A1}}{(\varepsilon^{v_1/v_T} + \varepsilon^{v_2/v_T})} \; ; \; I_S\left[\varepsilon^{-v_{x2}/v_T}\right] = \frac{I_{A2}}{(\varepsilon^{v_1/v_T} + \varepsilon^{v_2/v_T}} . \tag{6-39}$$

Substituting these last results into (6-38) yields

$$(I_1 - I_2) = \frac{I_{A1}(\varepsilon^{v_2/v_T} - \varepsilon^{v_1/v_T}) + I_{A2}(\varepsilon^{v_1/v_T} - \varepsilon^{v_2/v_T})}{(\varepsilon^{v_2/v_T} + \varepsilon^{v_1/v_T})} , \tag{6-40}$$

which can be rearranged into the form,

$$(I_1 - I_2) = (I_{A1} - I_{A2}) \frac{(\varepsilon^{v_2/v_T} - \varepsilon^{v_1/v_T})}{(\varepsilon^{v_2/v_T} - \varepsilon^{v_1/v_T})} \quad . \tag{6-41}$$

Now the voltage across diodes D_1 and D_2 cause currents I_{D1} and I_{D2} where

$$\left.\begin{aligned} I_{D1} &= I_S \, \varepsilon^{(v_c - v_1)/v_T} \\ I_{D2} &= I_s \, \varepsilon^{(v_c - v_2)/v_T} \end{aligned}\right\} \quad . \tag{6-42}$$

Taking logarithms,

$$\begin{aligned} v_1 &= v_c - v_T \ln(I_{D1}/I_S) \\ v_2 &= v_c - v_T \ln(I_{D2}/I_S) \quad . \end{aligned} \tag{6-43}$$

Substituting (6-43) into (6-41) delivers

$$(I_1 - I_2) = (I_{A1} - I_{A2}) \frac{(\varepsilon^{v_c/v_T})(\varepsilon^{-\ln(I_{D2}/I_S)} - \varepsilon^{-\ln(I_{D1}/I_S)})}{(\varepsilon^{v_c/v_T})(\varepsilon^{-\ln(I_{D2}/I_S)} + \varepsilon^{-\ln(I_{D1}/I_S)})}$$

$$= (I_{A1} - I_{A2}) \left[\frac{-I_{D2}/I_S + I_{D1}/I_S}{-I_{D2}/I_S - I_{D1}/I_S} \right]$$

or

$$(I_1 - I_2) = \frac{(I_{A1} - I_{A2})(I_{D2} - I_{D1})}{(I_{D2} + I_{D1})} \tag{6-44}$$

and since $I_{D1} + I_{D2} = I_0$

$$(I_1 - I_2) = \frac{(I_{A1} - I_{A2})(I_{D2} - I_{D1})}{I_0} \quad . \tag{6-45}$$

If $g_m R \gg 1$,

$$(I_1 - I_2) \approx \left[\frac{v_a v_b}{R_a R_b I_0}\right] , \tag{6-46}$$

which is the desired idealized multiplier output.

Using (6-21), (6-45) can be written as the product of two Taylor series.

$$(I_1 - I_2) = \frac{1}{I_0}\left(A_1 v_a + \frac{2A_3}{3!}(v_a/2)^3 + \frac{2A_5}{5!}(v_a/2)^5 + \ldots\right) X$$

$$\left(A_1 v_b + \frac{2A_3}{3!}(v_b/2)^3 + \frac{2A_5}{5!}(v_b/2)^5 + \ldots\right) \tag{6-47}$$

If $g_m R >> 1$,

$$(I_1 - I_2) \approx \frac{v_a v_b}{I_0 R_a R_b}\left[1 - \frac{2(v_a/2v_T)^2}{3(g_m R)^3} - \frac{2(v_a/2v_T)^4}{5(g_m R)^5} - \ldots\right] X$$

$$\left[1 - \frac{2(v_b/2v_T)^2}{3(g_m R)^3} - \frac{2(v_a/2v_T)^4}{5(g_m R)^5} - \ldots\right] \tag{6-48}$$

6.2.3 Circuit Comparisons

A comparison of the circuits in Figures 6-3 and 6-4 can be accomplished by studying their companion equations (6-30) and (6-48). The second order terms are $x_2 = (v_b/2v_T)^2/6$ in (6-30) and $y_2 = 2(v_b/2v_T)^2/3(g_m R)^3$ in equation (6-48). The ratio of the first to the second terms is $x_2/y_2 = (g_m R)^3/4$.

Table 6-1 lists some typical values of the higher order terms for the second circuit. For the second order term to be less than 0.01 or 1%, $(v_b/2v_T)$ must be less than 0.245 for the circuit of Figure 6-3 and 0.6928 for the circuit of Figure 6-4 when $g_m R = 4$. It can be seen that if $g_m R \approx 1000$, then $(v_b/2v_T)$ can be arbitrarily high (>170). It can be concluded that the circuit in Figure 6-4 can handle larger signals without distorting if $g_m R_a = g_m R_b > 1000$. These calculations for the multiplier were limited to steady state very low frequency input signals. The differential pairs are assumed to be perfectly

TABLE 6-1

$v/2v_T$	$(v_2/2v_T)^2/6$	$(v/2v_T)^4/120$	$(v/2v_T)^6/5040$
0	0	0	0
0.1	0.00166	8.33×10^{-17}	
0.245	0.01	3×10^{-5}	
0.5	0.04166	5.2×10^{-5}	
1.0	0.1667	0.0833	1.984×10^{-4}
2.0	0.6667	0.1333	0.01269
3.0	1.5000	0.675	0.1446

g_mR	$v/2v_T$	$2(v/2v_T)^2/3(g_mR)^3$	$2(v/2v_T)^4/5(g_mR)^5$	$2(v/2v_T)^6/7(g_mR)^7$
4	0.6928	0.01	1.8×10^{-4}	
4	1	0.0208	7.81×10^{-4}	
4	2	0.0833	0.125	0.00223
10	1.732	0.01	1.8×10^{-4}	
100	17.32	0.01	1.8×10^{-4}	
1000	173.2	0.01	1.8×10^{-4}	

matched and the current sources ideal. A nonideal current source principally effects the common mode signals, but not necessarily the differential nonlinearities that are calculated above.

7.0 DEMODULATOR CIRCUITS

Signal detection and demodulation are, of course, fundamental receiver requirements. While demodulator circuits abound in literature[24], most of the available circuits are not amenable to monolithic integration. The Costas loop demodulator offers numerous attributes that render its monolithic realization feasible and desirable. With minor modifications of its loop parameters, the Costas loop can be used for coherent demodulation of QPSK, PSK, PM, FM, and FSK signals. While the Costas loop has several alternative configurations, the configuration in Figure 7-1 was chosen as the one best suited for implementation in integrated circuit form and the one which takes best advantage of the capabilities of available IC components. Figure 7-2 shows the integrated circuit interconnect diagram for this configuration.

7.1 Costas Loop

Initial tradeoff studies considered two other realizations of the Costas loop. In the first, the VCO has two in-phase outputs, one of which is fed through a 90° phase shifter to the phase detector. Phase shifters generally employ transmission line techniques which are not suitable for integration. The second loop considered employs a VCO operating at twice the input frequency. The VCO has two inphase outputs which are fed into divide-by-two circuits. One of the dividers triggers on a positive slope and the other on a negative slope. This provides the desired quadrature outputs at the input frequency. This approach was rejected because it requires a significantly greater amount of circuitry than the chose configuration, and the VCO is difficult to build for very high frequency operation. The configuration of Figure 7-1 has none of the above mentioned disadvantages.

In the Costas loop of Figure 7-1, input signal is fed, via the RF amplifier, to each of the two phase detectors. If no input signal modulation is present, the input signal can be written in the steady state as

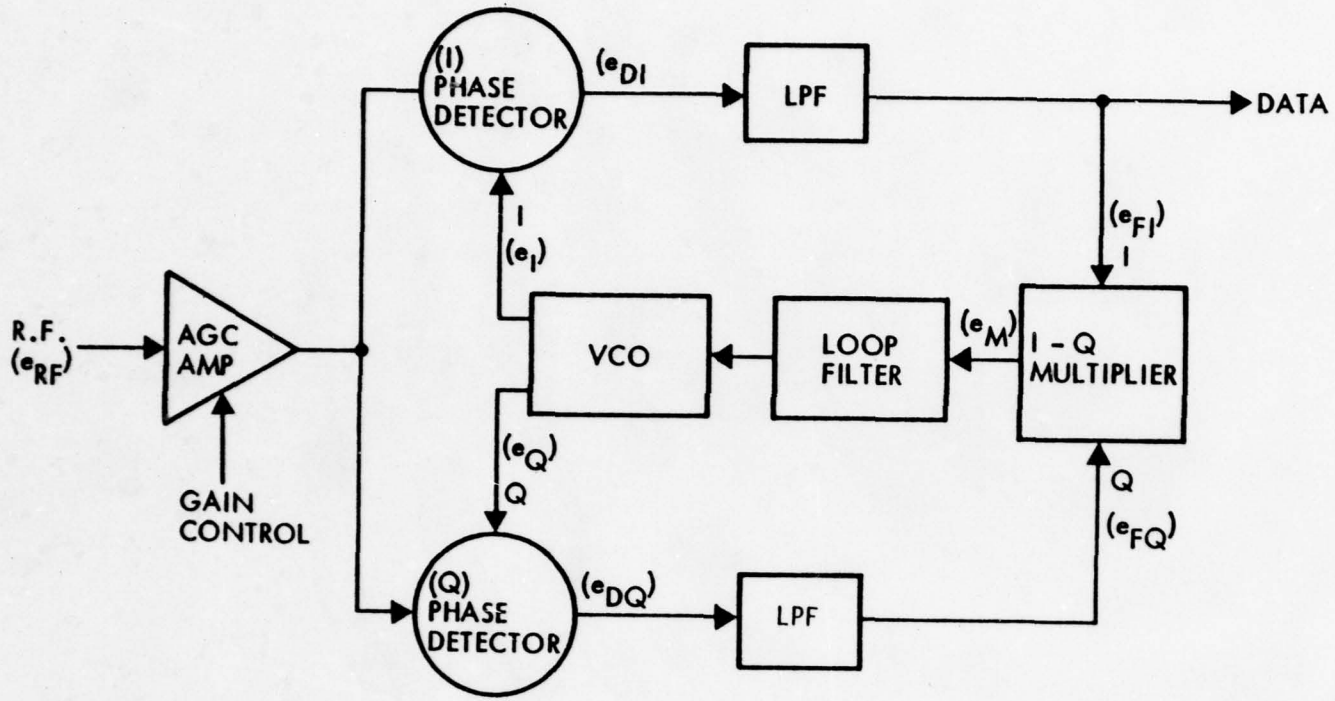

Figure 7-1 RFLSI Costas Demodulator
Symbols I and Q denote in-phase and quadrature signal components; symbol LPF connotes a low pass filter.

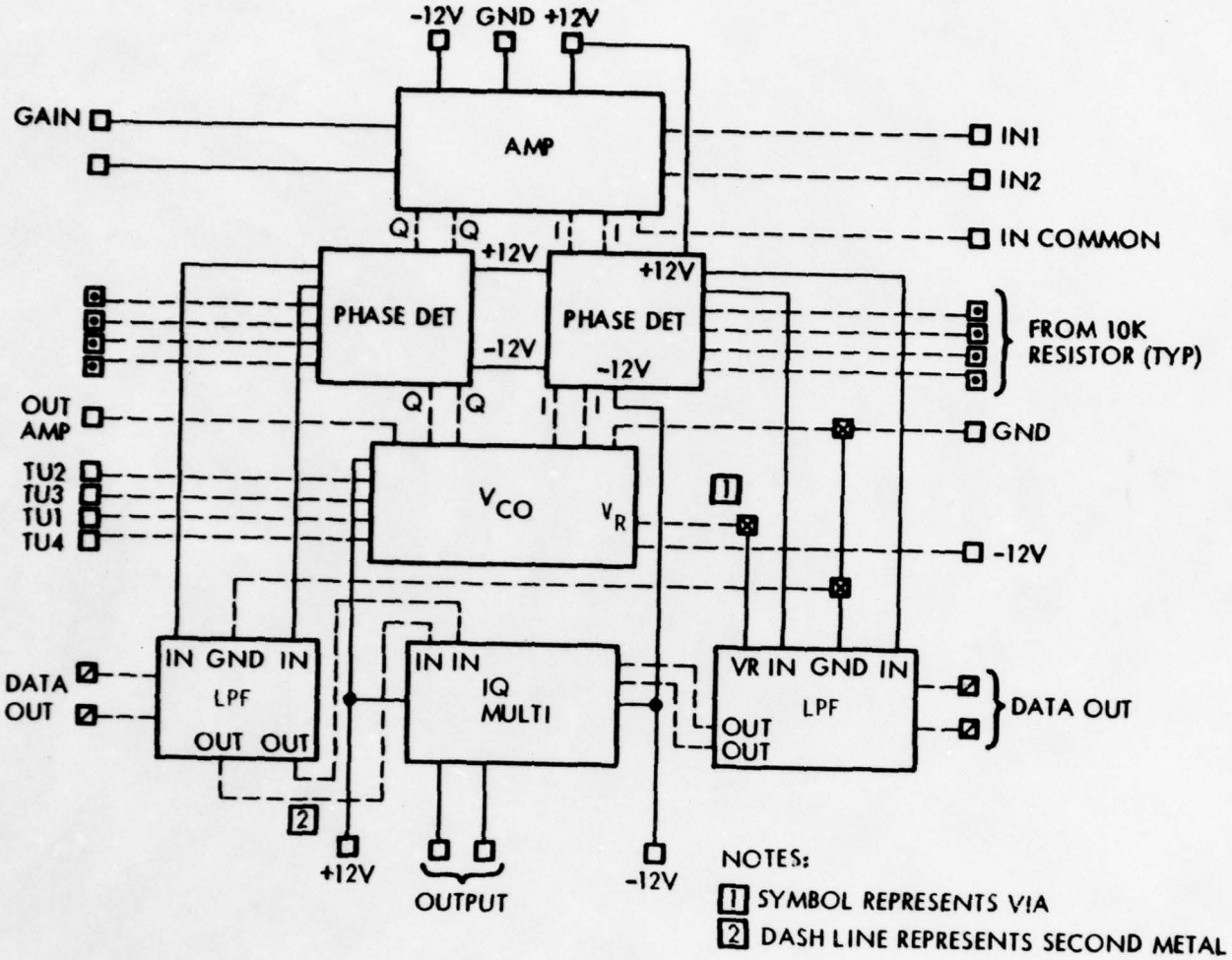

Figure 7-2 RFLSI Interconnect Diagram of Costas Loop

$$\varepsilon_{RF} = A \sin\omega_s t. \tag{7-1}$$

The VCO has two outputs which are at the same frequence, but 90° out out of phase with one another. Thus in Figure 7-1,

$$\varepsilon_I = B \sin \omega_o t, \tag{7-2}$$

$$\varepsilon_Q = B \cos\omega_o t, \tag{7-3}$$

The phase detectors are essentially linear multipliers or mixers. The in-phase detector output is

$$\varepsilon_{DI} = K_1 AB \cos(\omega_s - \omega_o)t - K_2 AB \cos(\omega_s + \omega_o)t, \tag{7-4}$$

and the quadrature phase detector output is

$$\varepsilon_{DQ} = -K_1 AB \sin (\omega_s - \omega_o)t + K_2 AB \sin(\omega_s + \omega_o)t, \tag{7-5}$$

where the K_i's are mixer proportionality constants.

The lowpass filters eliminate the higher frequency term so that the I-Q multiplier inputs are

$$\varepsilon_{FI} = K_1 A_B \cos \omega_\beta t \tag{7-6}$$

$$\varepsilon_{FQ} = -K_1 AB \sin \omega_\beta t, \tag{7-7}$$

with

$$\omega_\beta = \omega_s - \omega_o \quad . \tag{7-8}$$

The I-Q multiplier is also essentially a mixer and thus,

$$\varepsilon_M = K_3' \varepsilon_{FI} \varepsilon_{FQ} = K_3 \sin 2\omega_\beta t \ . \tag{7-9}$$

Voltage ε_M represents the error signal, scaled by the loop filter, which drives the voltage controlled oscillator (VCO) in the direction of

frequency locking at the input frequency, provided only that $2\omega_\beta$ is within the loop bandwidth. The VCO is either swept or manually tuned until $2\omega_\beta$ is within the loop bandwidth, at which point the loop pulls in automatically. The phase locking mechanism can be understood by substituting a phase error termed (ϕ) for $\omega_\beta t$ in equations (7-6) through (7-9). The I-Q multiplier inputs become

$$\varepsilon_{FI} = K_1 A_B \cos \phi \tag{7-10}$$

$$\varepsilon_{FQ} = K_1 AB \sin \phi \tag{7-11}$$

and its output is

$$\varepsilon_M = K_3 \sin 2\phi \tag{7-12}$$

which drives the VCO in the direction of phase locking. It can be seen from above that phase locking in the sense of $\varepsilon_M = 0$, can occur either at $\phi = 0$ or $\phi = \pi$. This reveals the basic ambiguity of the Costas loop, i.e., it is not known a priori whether the loop locks in-phase or 180° out of phase with respect to the incombing signal. The resolution of this ambiguity is discussed shortly.

The assumption thus far is that there is no data carried by the incoming signal. Removing that assumption, the incoming signal to which the VCO has phase locked can be represented by

$$\varepsilon_{RF} = A \sin(\omega_s t + \Theta) \tag{7-13}$$

where Θ has two permitted values, 0 and π. Equation (7-4) which describes the in-phase detector output becomes, assuming locked phase,

$$\varepsilon_{DI} = K_1 AB \cos [(\omega_o - \omega_o)t + \Theta] - K_2 A_B \cos [(\omega_o + \omega_o)t + \Theta] \tag{7-14}$$

which reduces to

$$\varepsilon_{DI} = K_1 A_B \cos \Theta - K_2 A_B \cos (2\omega_o t + \Theta). \tag{7-15}$$

The dc term ($K_1AB \cos \Theta$) corresponds to the data. Since Θ can only take on the values 0 and π, the dc term is always

$$\bar{\varepsilon}_{DI} = \pm K_1 A_B. \tag{7-16}$$

The question as to whether the output data stream is the correct data or the complement of the correct data is resolved by having the data stream start with a known initial code. If the output data is the complement of the known code, it is inverted, removing the ambiguity.

7.2 Voltage Controlled Oscillator

The voltage-controlled oscillator (VCO) required of the Costas loop demodulator must satisfy numerous requirements. First and foremost, it must supply quadrature outputs. Second, the VCO output signal frequency must be a nearly linear function of VCO input control voltage. Third, the amplitude of sinusoidal oscillation should be reasonably constant over the range of receiver input signal frequencies. Finally, the frequency of VCO oscillation should be as stable as possible throughout the anticipated range of thermal and other environmental conditions.

7.2.1 VCO Limitations[25]

A monolithic VCO suffers from the limitation that its frequency determining elements are determined by voltage controlled resistance, voltage controlled capacitance, or current-controlled active element parameters. Voltage variable or "pinch" resistors suffer from numerous on-chip coupling parasitics which render them difficult to match. Voltage variable capacitances demand special integrated circuit processing steps in order to achieve reasonable linear and broad tuning range capabilities. Active element control, such as the control of transistor gain-bandwidth product, f_T, in biasing regimes where f_T is a nominally linear function of collector current, suffers from inherent thermal sensitivity problems.

7.2.2 VCO Circuit

Although there are numerous VCO configurations[26]-[28], most of the available circuits are not capable of producing quadrature outputs and most of the classical configurations are not capable of producing minimally distorted sinusoidal oscillations at the RF frequencies indigenous to the GPS receiver. One circuit, which has demonstrated proven capability to about 1 GHz is shown in Figure 7-3. Since transistors Q_3 and Q_4 have a common current source, oscillations in Q_4 must be 180° out of phase with those in Q_3. A similar argument applies to Q_5 and Q_6. The VCO oscillates at a frequency such that the total phase shift through the four stages is 360°. Since the phase difference bewteen Q_3 and Q_4 is 180°, this situation forces the phase difference between Q_3 and Q_5 to be 90% and between Q_4 and Q_6 to be 90°, thus guaranteeing that the two outputs are always in quadrature.

Tuning is accomplished via two mechanisms. If Q_7 is considered to be a voltage variable resistor, then the oscillation frequency is determined by the time required to charge the RC network made up of Q_7 and the capacitors in its collector and emitter. The tuning mechanisms are then obvious. The first is to vary the value of the R by changing the bias applied to the base of Q_7. The second is to vary the amount of current available to charge the RC network by varying the bias applied to the base of Q_1.

The same argument applies to the Q_2 - Q_5 - Q_6 - Q_8 combination. By combining both tuning mechanisms it was possible to tune the VCO over a wide range of RF frequencies. In actual operation, the Q_1 - Q_2 base voltage is used to set the oscillation frequency and Q_7 - Q_8 accomplish tuning. Transistors Q_9 through Q_{12} isolate the tuning circuit from the external load. Resistors labeled R from a divider network with the external load, thereby reducing the VCO output voltage to appropriate levels.

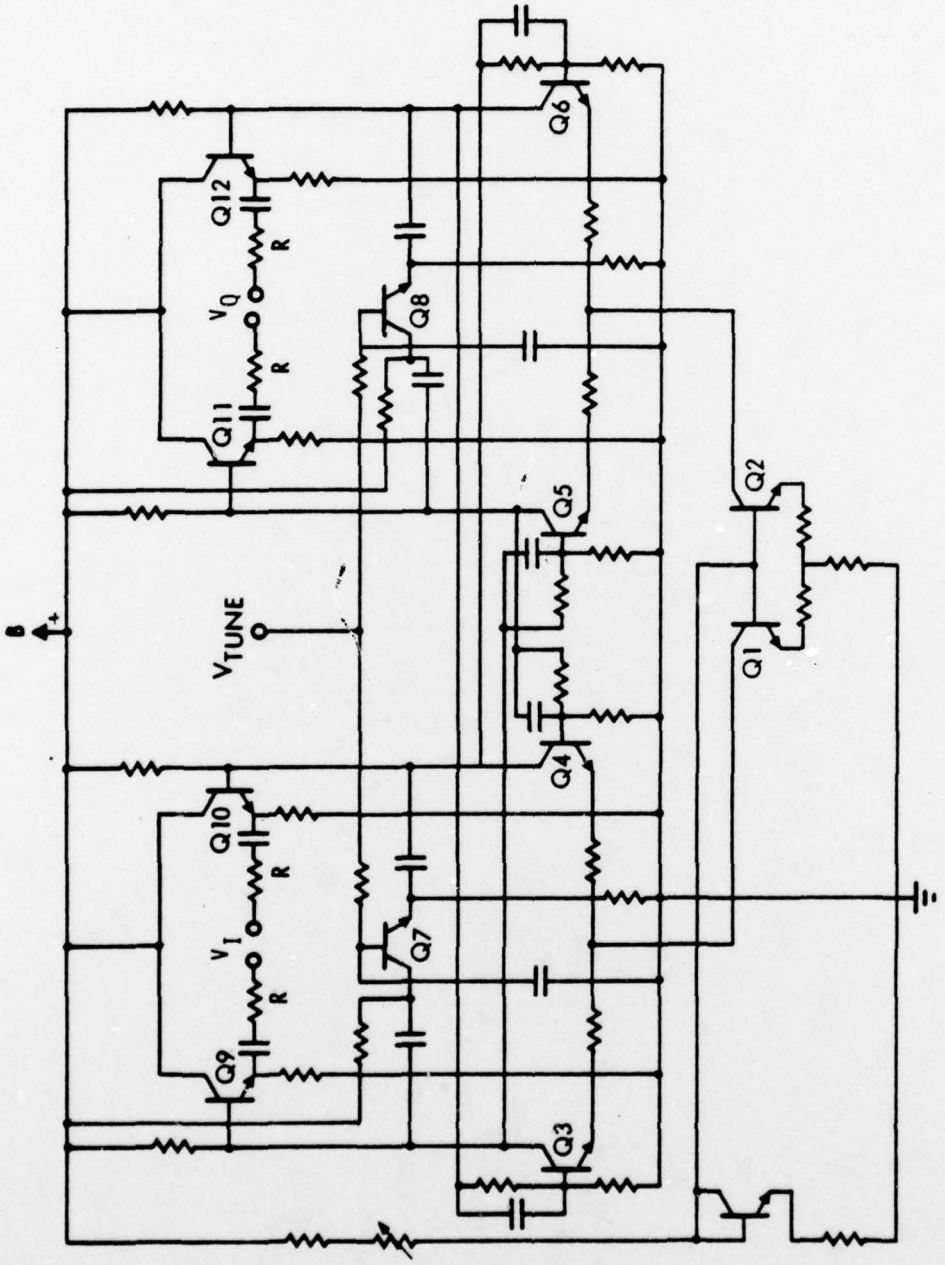

Figure 7-3 Voltage Controlled Oscillator with Quadrature Output Capability

7.2.3 Quadrature Frequency Doubler

The present expertise in circuit design allows for a quadrature VCO operating to about 1 GHz using only transistors and resistors, and to about 2 GHz if lossless matching networks are used. The L-C matching networks are quite wasteful of silicon area, they complicate layout, and their performance is far less than ideal. If quadrature double frequency sinusoids can be conveniently generated, the frequency range for VCO operation without bulky matching networks may extend to 2 GHz, and the ultimate frequency of a monolithic Costas loop might approach 4 GHz if matching networks are used.

The generation of the quadrature double frequencies appears straight-forward, if one remembers that

$$\left.\begin{aligned} \sin 2\omega t &= 2\omega \sin\omega t \cos \omega t \\ \cos 2\omega t &= \cos^2\omega t - \sin^2\omega t \end{aligned}\right\} . \qquad (7\text{-}17)$$

These equations can be implemented as shown in Figure 7-4. The $2[\sin\omega t \cos \omega t]$ term is implemented by summing the outputs of two mixers - one which has its upper level driven by $\sin \omega t$ and the lower by $\cos \omega t$, and the other with $\cos \omega t$ on the upper level and $\sin \omega t$ on the lower level. The $\cos^2\omega t - \sin^2\omega t$ is obtained similarly from mixers with inputs of $\cos \omega t$ and $\cos \omega t$, and of $\sin \omega t$ and $-\sin \omega t$. This arrangement has several advantages. First, the four mixers are all identical. Second, two outputs of the VCO are equally loaded so that the quadrature output relationship can be preserved. Finally, the effect of a phase difference between the upper and lower inputs of the mixers is cancelled. If there is a phase differential Θ between the two paths A and B in Figure 7-5, the outputs of the circuit in Figure 7-1 will be $\sin(2\omega t + \Theta)$ and $\cos(2\omega t + \Theta)$, thus preserving the desired quadrature relationship.

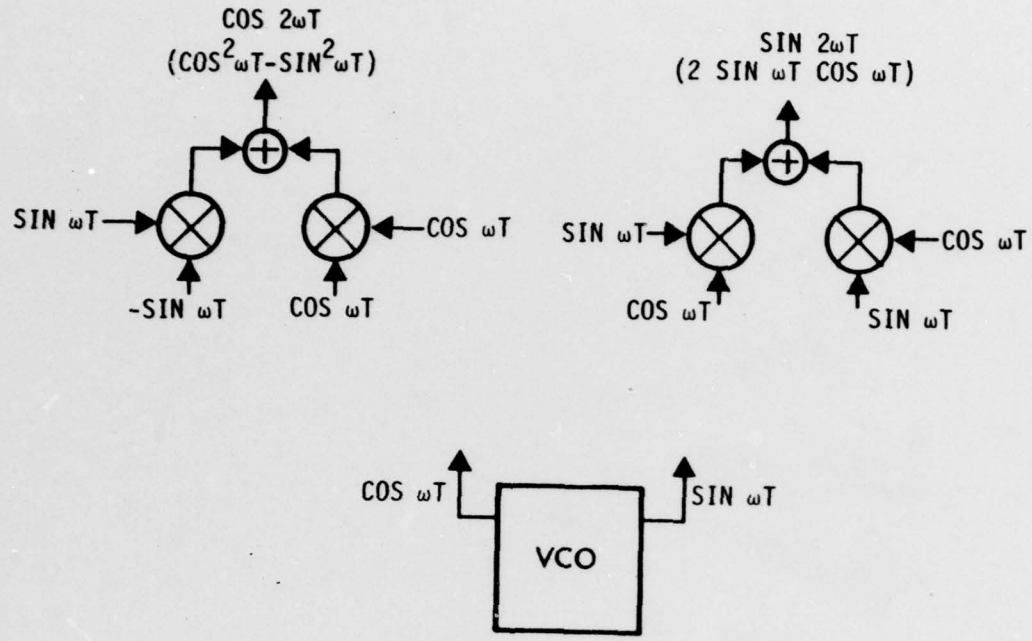

Figure 7-4 System Realization of Quadrature Frequency Doubler

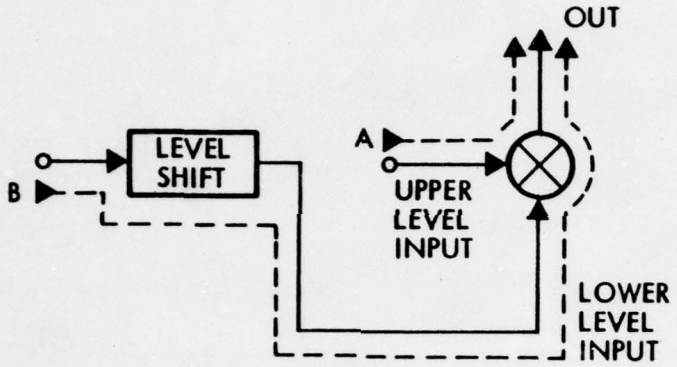

Figure 7-5 Signal Paths through Mixer which may cause undesired phase shifts

In practice, each of the quadrature outputs at the desired frequency usually drives one mixer. In this case, the best circuit arrangement is probably to directly utilize the current output at frequency 2ω as an input to a third mixer level, using a circuit as shown in Figure 7-6. In this suggested circuit, it can be shown that V_{OUT} is proportional to $\cos(2\omega t)$ if the input of A is $\sin\omega t$, the input at B is $-\sin\omega t$, and the inputs at both C and D are $\cos\omega t$. On the other hand, if A and D are driven by sinusoids and B and C are excited by cosinusoids, the output voltage is proportional to $\sin(2\omega t)$.

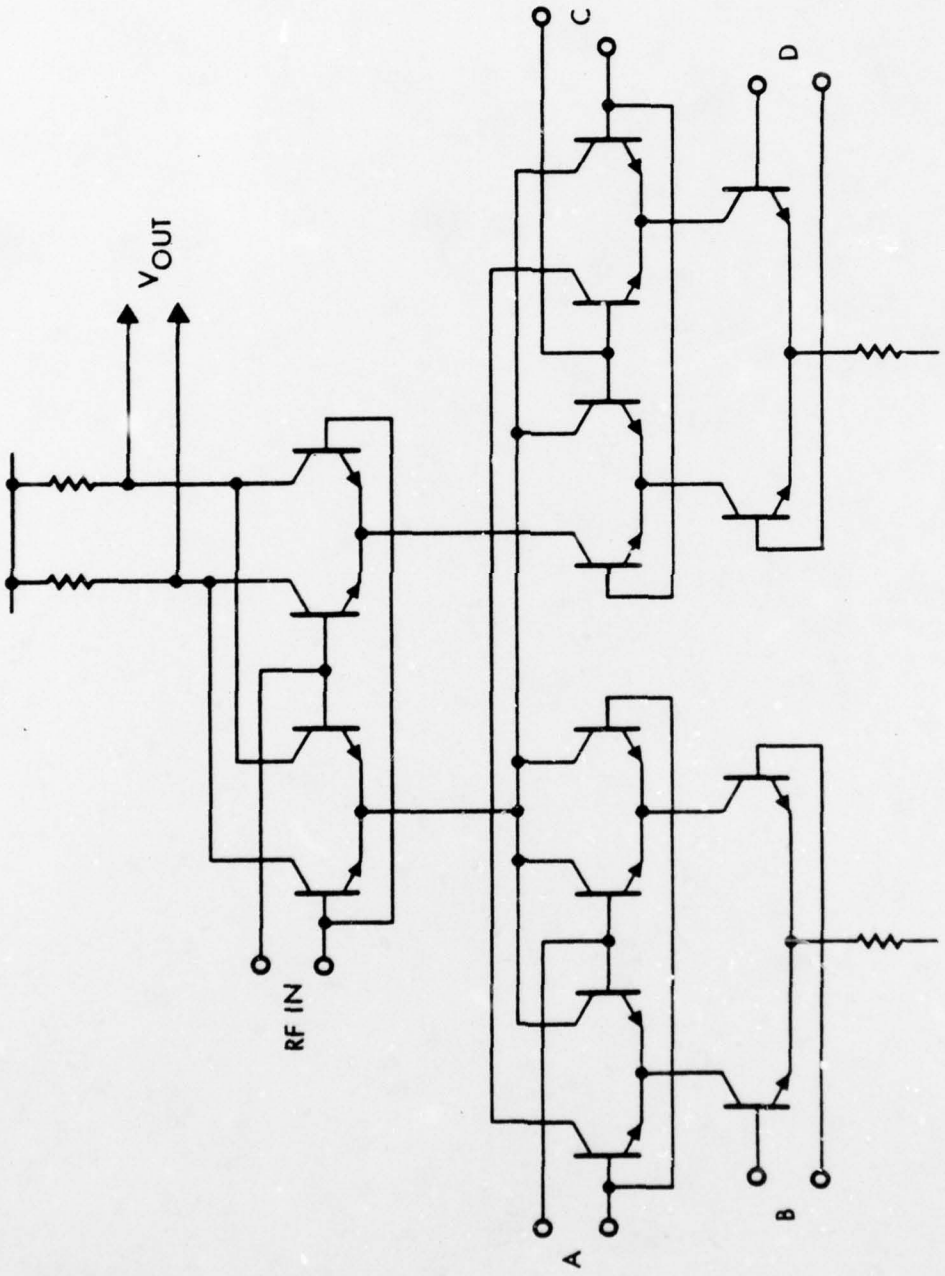

Figure 7-6 Practical Quadrature Doubler Circuit using a Modified 3-Level Mixer

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